CURRICULUM VITAE

PERSONAL INFORMATION

Name **LORENZI, Paolo**

Address

Telephone

E-mail

Nationality Italian

Date of birth FEBRUARY 7, 1982

WORK EXPERIENCE

• March 2011 – Until now (2013)

*"**Research Collaborator**" (Assegnista di Ricerca) at the Dipartimento di Ingegneria Elettronica - "La Sapienza" University of Rome to perform "**Nanoelectronic memories**".*
The subject of the work focused on electrical characterization and modeling of resistive memory cells.

• October 2009 – January 2011

*"**Ph.D. Student**" at the CEA/LETI/MINATEC of Grenoble, France, in collaboration with the Institut National Polytechnique de Grenoble (INPG) to perform "**Resistive memory cells for intelligent circuit application.**"*
The subject of the work focused on the electrical characterization of dielectric, semiconductor and metal films for application in CMOS microelectronics.

• February 2009 - May 2009

*"**Research Collaborator**" at the Dipartimento di Ingegneria Elettronica - "La Sapienza" University of Rome to perform "**Workbench setup for the automation of data retention measurements in TANOS flash memories**."*
The work focused on the electrical characterization, analysis and modelling of semiconductor memories.

• October 2008 – January 2009

*Engaged as "**Research Collaborator**" at the Dipartimento di Ingegneria Elettronica - "La Sapienza" University of Rome to perform "**Pulse programming algorithms for new generations NAND memory cells.**"*
The project focused on the electrical characterization of high-k dielectrics for memories applications.

• September 2005 – August 2006

Collaborator at library of Dipartimento di Fisica Tecnica – "La Sapienza" University of Rome

• September 2002 – August 2004

Collaborator at admission office of Corso di laurea Ingegneria Elettronica – "Roma Tre" University of Rome

PUBLICATIONS

• 2013

***"Impact of the forming conditions and electrode metals on read disturb in HfO2-based RRAM",** P. Lorenzi, P; R. Rao; F. Irrera; Microelectronics Reliability, 2013, in press*

• January 2013

***"Forming Kinetics in HfO2 - Based RRAM Cells"**, P. Lorenzi, P; R. Rao; F. Irrera; Electron Devices, IEEE Transactions on , vol.60, no.1, pp.438-443, Jan. 2013*

• May 2012 (Milan, IT)

*"**Impact of Forming Pulse Geometry and Area Scaling on Forming Kinetics and Stability of the Low Resistance State in HfO2-Based RRAM Cells**," P. Lorenzi; R. Rao; F. Irrera, International Memory Workshop IMW 2012*

• *December 2011 (USA)* — *"**Experimental and Theoretical Study of Electrode Effects in HfO2 based RRAM**", C. Cagli, J. Buckley, V. Jousseaume, T. Cabout, A. Salaun, H. Grampeix, J. F. Nodin, H. Feldis, A. Persico, J. Cluzel, P. Lorenzi,L. Massari,R. Rao, F. Irrera, F. Aussenac, C. Carabasse, M. Coue, P. Calka, E. Martinez, L. Perniola, P. Blaise, Z.Fang, Y. H. Yu, G. Ghibaudo, D. Deleruyelle, M. Bocquet, C. Müller, A. Padovani, O. Pirrotta, L. Vandelli, L. Larcher, G. Reimbold, B. de Salvo;* IEDM 2011

• *April 2011* — ***"Comparative study of non-polar switching behaviors of NiO- and HfO2-based oxide resistive-RAMs"** V. Jousseaume, A. Fantini, J.F. Nodin, C. Guedj, A. Persico, J. Buckley, S. Tirano, P. Lorenzi, R. Vignon, H. Feldis, S. Minoret, H. Grampeix, A. Roule, S. Favier, E. Martinez, P. Calka, N. Rochat, G. Auvert, J.P. Barnes, P. Gonon, C. Vallée, L. Perniola, B. De Salvo, Solid-State Electronics, Volume 58, Issue 1, April 2011, Pages 62-67*

• *December 2010 (San Diego, USA)* — *"**A study of the HRS and LRS temperature behavior of Pt/HfO2/Pt based Oxide Resistive RAM**", Lorenzi P., Singh P., Buckley J., Jousseaume V., Nodin J-F., Grampeix H., Persico A., Betti Beneventi G., Tirano S., Perniola L., De Salvo B.; SISC 2010*

• *May 2010 (Seul, Korea)* — *"**Comparative study of non-polar switching behaviors of NiO- and HfO2-based Oxide Resistive-RAMs** ", Jousseaume, V.; Fantini, A.; Nodin, J.F.; Guedj, C.; Persico, A.; Buckley, J.; Tirano, S.; Lorenzi, P.; Vignon, R.; Feldis, H.; Minoret, S.; Grampeix, H.; Roule, A.; Favier, S.; Martinez, E.; Calka, P.; Rochat, N.; Auvert, G.; Barnes, J.P.; Gonon, P.; Vallee, C.; Perniola, L.; De Salvo, B.; Memory Workshop (IMW), 2010 IEEE International*

• *March 2010 (Glasgow, UK)* — *"**Advanced Characterization of Metal/High-k Interface**", F. Irrera, P. Lorenzi, R. Rao, R. Simoncini, G. Ghidini, H.D.B. Gottlob, M. Schmidt; ULIS 2010*

• *March 2010* — *"**Electron-Related Phenomena at the TaN/Al2O3 Interface** ", Rao, R.; Lorenzi, P.; Ghidini, G.; Palma, F.; Irrera, F., Electron Devices, IEEE Transactions on, Volume: 57 , Issue: 3 , 2010*

• *July 2009 (Genova, IT)* — *"**Charge trapping NanoElectronic memory**", Lorenzi, P. Rao, R. Palma, F. Irrera, F. Ghidini, G. Dipt. di Ing. Elettron., Univ. La Sapienza, Rome, Italy, Nanotechnology, 2009. IEEE-NANO 2009. 9th IEEE Conference on*

• *October 2009* — *"**Charge Trapping Non Volatile Memory**", Paolo Lorenzi, Rosario Rao, Gabriella Ghidini, Fabrizio Palma, and Fernanda Irrera, ECS Transactions. 25 (7), 269 (2009)*

• *January 2006* — *"**Programmable analog circuits yield single-chip sinusoidal oscillators**", S. Salvatori, P. Lorenzi, EDN: Information, News, & Business Strategy for Electronics Design Engineers, 19/1/2006, http://www.edn.com/contents/images/6298269.pdf*

EDUCATION AND TRAINING

• *July 2008* — ***Master's Degree in Electronic Engineering** at "La Sapienza" University of Rome.*

*Mark: **110/110 cum laude***

***Thesis**: "Analysis and characterization of Flash memories with high-k IPD."*

• *December 2004* — ***Bachelor's Degree in Electronic Engineering** at "Roma Tre" University of Rome.*

*Mark: **110/110 cum laude***

***Thesis**: "Analysis and characterization of programmable analog devices".*

• *July 2001* — ***High School Degree** at "Antonio Labriola" Liceo Scientifico Statale of Rome.*

*Mark: **100/100***

PERSONAL SKILLS AND COMPETENCES

MOTHER TONGUE **ITALIAN**

OTHER LANGUAGES

ENGLISH

- *Reading skills* Excellent
- *Writing skills* Good
- Verbal skills Excellent

FRENCH

- *Reading skills* Excellent
- *Writing skills* Good
- Verbal skills Excellent

TECHNICAL SKILLS AND COMPETENCES

Clean Room: continual permanence in a **100/10 class clean room** at CEA/LETI (Grenoble) of 8.000m^2 of surface **following the technology process flow** of microelectronic wafer lots.

Microscopy: performing **SEM (Scanning Electron Microscopy) in-line observations on MEB 5000 and MEB 4160** on entire or cut wafers to observe depositions thicknesses, material adhesion and check the results of particular processes steps.

Electrical characterization: knowledge of the laboratory electrical measurements techniques for steady-state and transient characterization of semiconductor electronic devices. In particular, matured skills in performing: **current-voltage, current-time, current-temperature** measurements; **pulsed C-V** for monitoring trapping and detrapping transients in defected oxides and semiconductors; **solid-state device modeling** finite element TCAD; **characterization and modeling of conduction mechanism** in oxides and semiconductors. Matured skills in the usage of the principal characterization laboratory equipments: **electrometers, LCR meters, pulses generators, oscilloscopes, semiconductor parameter analyzers**.

Knowledge of automation and simulation software **Labview**

Knowledge of numerical analysis tools **Matlab** and **Mathcad**

Knowledge of programming and hardware description languages: **Java, C, HTML, VHDL, Assembler**.

Knowledge of circuital simulation software: **Orcad Spice, NgSpice**.

Knowledge of operating systems and principal office software: **Microsoft Windows, Linux, Microsoft Word, Power Point, Excel, KaleidaGraph, Origin.**

ORGANIZATIONAL SKILLS AND COMPETENCES

Team work and coordination of activities driven by problem solving issues. Capability to work with heterogeneous kind of professionals in order to reach common targets.

DRIVING LICENCE(S)

European Car (B).