Open Research Position

"Design and Implementation of New Signal Waveforms and Processing Techniques for a Lower Energy Consumption "

We are offering a full-time research scientist (postdoctoral/experienced engineer) position in the area of digital communications with a particular emphasis on adaptive radio access systems (single carrier and multi-carrier) and implementation on USRP platforms.
Proposed research work has received a French government support granted to the CominLabs excellence laboratory and managed by the National Research Agency in the "Investing for the Future" program under reference ANR-10-LABX-07-01

Areas of interest:

We are looking for candidates with experience and knowledge on: digital communication systems more specifically on physical layer aspects related to the design and implementation of transmission and reception blocks, and skills with experience on hardware implementation on USRP platforms. Skills with experience using DSP and FPGAs with knowledge on C++ and /or Python programming may be very advantageous. Besides the applicant must:

1) Have excellent oral and writing in English.
2) Have EE engineering with experience on embedded electronic disciplines or a Ph.D. degree in EE.
3) Have a strong digital communications background.
4) Have already demonstrated research performance and capabilities by publications and patents.

For no French educated candidates, French speaking and/or writing is not required but may be advantageous.

The work of the candidate will consists in

1. Comprehension and mastery of proposed new modulation scheme for low energy consumption.
2. Develop proposed modulator, with appropriate precoding scheme using USRP platforms.
3. Develop the corresponding demodulator including the synchronization / equalization / and the channel estimation stage, using USRP platform.
4. The overall proposed communication system must be tested under real situation.

Employment: The research grant is awarded for **18 months** and its yearly amount is about 46.884,00 € gross. The position will take place at the IETR (Institute of Electronic and telecommunications of Rennes) in the **SCEE** (Signal, Communication & Embedded Electronics) research group of CentraleSupélec engineering school in campus of Rennes (France). Expected starting is: **1st January 2019**.

Application: Interested candidates should contact: Jacques Palicot <jacques.palicot@centralesupelec.fr>, Carlos Faouzi Bader <faouzi.bader@supelec.fr>, and Yves Louët <yves.louet@centralesupelec.fr >by sending a detailed CV, graduate transcript(s), representative publications, statement of research experience and interests, and two references.

We may contact interesting candidates once we receive the application. Therefore, please submit your application as early as possible. Application deadline: **September 2018.**