ANDREA VICI

Personal Informations

Born in Rome, Italy, 30 May 1992

E-mail ndr.vici@gmail.com

Skype andrea_vici

Work Experience

Mar – Sept 2018 LFoundry a Smic Company — Avezzano (Aq)

***Internship** for Master's degree thesis*

Thesis: *Study of peripheral MOSFET gate oxides traps in Back-Side Illuminated CMOS Image Sensors*
Electrical characterization of interface and near-interface traps in Si/SiO_2 systems for Back-Side Illuminated CMOS Image sensors (technological node 110 nm).
Reference: Felice Russo · felice.russo@lfoundry.com

Mar – Sept 2015 Gelatorino — London (UK)

Ice Cream maker

Sales assistant

Education

2015-2018 Sapienza University of Rome

*MSc in **Nanotechnology Engineering***

Mark: 110/110 cum laude
Curriculum: *Electronics and Photonics*
Thesis: *Study of peripheral MOSFET gate oxides traps in Back-Side Illuminated CMOS Image Sensors*
Description: a systematic characterization of the traps in the Gate Stacks of CMOS Image Sensors using Charge Pumping (CP) and Low Frequency Noise (LFN) techniques has shown that donor-like border traps are responsible for the limited lifetime in the Back-Side Illuminated (BSI) configuration respect to the Front-Side Illuminated (FSI) one of the same technological node (110=nm)
Advisors: Prof. Fernanda Irrera, Dr. Felice Russo & Eng. Nicola Lovisi

2011-2015 Sapienza University of Rome

*BSc in **Clinical Engineering***

Mark: 109/110
Thesis: *Optimization of the geometry of a thin film heater for Lab-On-Chip applications*
Description: design of a Cr/Al/Cr thin film heater through AutoCAD and Comsol Multiphysics® and its realization in the dedicated laboratory of the *Dipartimento di Ingegneria Elettronica e Telecomunicazioni* (DIET) using photo-lithographic, etching and physical vapor deposition techniques
Advisor: Prof. Domenico Caputo

2006-2011 Liceo Scientifico Augusto Righi — Rome

High School Diploma

Rank: 87/100
Scientific High School
Bilingual section (French/English)

Publications

2018

64th International Electron Devices Meeting

Title: *Through-silicon-trench in back-side-illuminated CMOS image sensors for the improvement of gate oxide long term performance*
Authors: A. Vici, F. Russo, N. Lovisi, L. Latessa, A. Marchioni, A. Casella, F. Irrera
Accepted for oral presentation at the 2018 International Electron Devices Meeting (IEDM) in San Francisco, USA

Laboratory Skills

Characterization techniques: *I-V measurements, C-V measurements, Charge Pumping, Spectroscopic Charge Pumping, Multi Frequency Charge Pumping, Negative Bias Temperature Instabilities, Flicker Noise, Random Telegraph Noise, Time Dependent Defect Spectroscopy*
Semiconductor characterization hardware tools: *Agilent B1500A Semiconductor Device Parameter, Keysight E4727A Advanced Low-Frequency Noise Analyzer, Pulse generators, Oscilloscopes, Probe stations*
Semiconductor characterization soft tools: *Synopsys Sentaurus TCAD, Comsol Multiphysics®, Boise State Band Diagram program*

Computer Skills

LaTeX, OpenOffice, Linux, Microsoft Windows, Labview, Matlab, AutoCAD

Other Informations

Driving Licenses

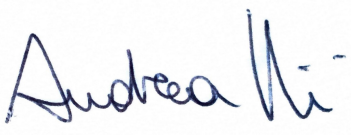
Category B and A3

Languages

- Italian · Mothertongue
- English · Intermediate (conversationally fluent)
- French · Intermediate (conversationally fluent)

Rome, 15/02/2018

Signature



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