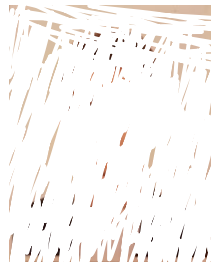


Abdallah Cheikh



Education	PhD Candidate in Ingegneria Elettronica - Expected to get the PhD degree by February/2020 at La Sapienza Roma Italia MS in Electrical Engineering - Graduated in 10/05/2016 at Rafik Hariri University RHU Lebanon (overall GPA: 85 / 100) BS in Electrical Engineering - 07/07/2014, Rafik Hariri University RHU (HCU) Lebanon Lebanese Baccalaureate - June 2011, Life Sciences - Graduated school from "Ras Beirut International School"
Professional Work/ Research Experience	- October 2018 – June 2019 RTL design and verification researcher at <i>Barcelona Supercomputing Center BSC on the European Processing Initiative Project EPI</i> - March 2016 – April 2016 Trainee as an electro-mechanical engineer at <i>Bassoul-Heneine s.a.l. (BMU, Renault, Alpha Romeo Agent in Lebanon)</i> - July 2015 – August 2015 <i>Internship as an electrical inspector on a construction site for Khatib & Alami (K&A)</i> - May 2014 – July 2014 Internship at a factory for electric power line production (low, medium, high voltage KV) at <i>National Cable Industry (NCI) Sharjah, United Arab Emirates (UAE)</i>
Research Experience	- Digital Logic RTL design Profound experience in RTL design both in VHDL and SystemVerilog. (3 plus years) Designed a pipelined interleaved multithreaded Processor named "Klessydra" Designed a special purpose vector accelerator for accelerating computations in Deep Convolutional Neural Networking (DCNN) applications. Integrated the core inside the Pulpino SoC from ETH-Zurich

Early works include hardwiring a 4-bit processor from logic gates only. (2014)

- **FPGA Synthesis and Verification**

Have lunched throughout my PhD career an extensive amount of FPGA synthesis for testing my Klessydra core, in which I used to fix error, latches, combinational loops, also mitigate timing delays, and on board dynamic power consumption.

- **Assembly Language (Risc-V)**

Throughout my career I wrote a huge set of programs/libraries in assembly. Partly to test some instructions, others to create a firmware for my core, and others are used as custom C libraries for Klessydra.

- **Testing and Verification**

Extensive experience in Design Verification with Modelsim or Questasim, and writing higher order verification tests in C. Not to mention FPGA synthesis verification in Vivado.

- **Microcontrollers/FPGA**

During my bachelors and my Masters degree I acquired skills working with the following:

MicroPIC 16F877A: was the first microcontroller I learned, mainly used for interfacing a wide range of sensors (Temperature, humidity, Ultrasonic, light, smoke)

Arduino UNO+MEGA: was used to do a line following robot, and also my BS project which used two Arduino microcontrollers connected wirelessly for detecting any electrical power theft. (Wireless power theft detection)

FPGA Xilinx Spartan-3E XC3S500E

Github Repos

- <https://github.com/klessydra/T02x>
- <https://github.com/klessydra/T03x>
- <https://github.com/klessydra/T13x>

Computer Skills

- *RTL design languages: (VHDL – SystemVerilog)*
- *Computer Programming Languages: C/C++*
- *Compute Scripting Languages: Shell, C-Shell, Tcl, MAKE, and CMAKE.*
- *Electronics Engineering synthesis-verification software: Modelsim, Questasim, Xilinx Vivado, and ISE.*
- *Electrical Engineering Software: Eagle – NI MultiSim – NI LabView - MATLAB*
- *Design Software tools: AutoCAD (2D drawing) - Adobe Illustrator*
- *Operating Systems: Linux Debian(Ubuntu), Microsoft Windows.*
- *Office Programs: MS Office package, LibreOffice,*
- *Basic Web Design Experience: HTML, CSS, Javascript.*

Languages

- Fluent in Arabic
- Fluent in English
- Fluent in Italian
- Working Knowledge in Spanish
- Basic/Fair knowledge in French

Conferences attended

- 2014 Mediterranean Gas & Oil International Conference
- 2017 New Generation of CAS (NGCAS)
- 2017 Applications in Electronics Pervading Industry Environment and Society (ApplePies)
- 2018 SIE Societa Italiana Di Elettronica
- 2019 Applications in Electronics Pervading Industry Environment and Society (ApplePies)

Workshops

- Risc-V workshop Barcelona 2018
- Risc-V workshop Zurich 2019
- Association for Computing ACM Europe Summer School 2019

References

- Available upon Request