EDUCATION

2016-2018: Special Master in Aerospace Engineering *(2 years)*
Sapienza University of Rome -Scuola Di Ingegneria Aerospaziale (SIA), Rome.
The learning objective is training experts that can be employed in advanced research and development centers in aerospace engineering.

2014: Engineering degree in Electronic Systems and Telecommunications *(3 years)*
Moulay Ben Abdellah University, Faculty of Sciences and Technologies, Fez.
Computer networks and information technology, design and installation of electronic and telecommunication systems.

2011: "Classes préparatoires aux grandes écoles" *(2 years)*
Electrical engineering, Oujda.

2009: High School *(12 years)*
Electrical Science, Technical High School, Taza.

PROFESSIONAL EXPERIENCES

Present: Assegno Di Ricerca Progetto "SIA-ASI-Development and integration of the Star sensor Image Processing Unit (SIPU) for the SPOT payload"

The Star sensor image on-board Processing for orbiting Objects deTection (SPOT) fits in this field as an innovative space based autonomous and versatile system for Resident Space Objects' optical detection via star sensors and for different Earth orbits scenarios. The project is being conducted in collaboration with the Italian Space Agency.

The main task is to develop, test, and implement the SPOT algorithms and interfaces on SoC/FPGA.

2020: Borsa Di Studio Ricerca Progetto "SIA-I.E.S. Hirempro-Development of the on-board computer based on FPGA for picosatellites (STECCO)"

STECCO (Space Travelling Egg-Controlled Catadioptric Object) is a nanosatellite composed by 6 PocketQube units (5x5x5 cm3) with a total mass of 0.85 kg and an envelope of 5x5x30 cm3.
https://sites.google.com/uniroma1.it/stecco-sia/home?authuser=0

I was Responsible for:

- The development, tests, and integration of an OBC based on SRAM-FPGA.
- Design, implementation, and test the flight software of STECCO.
- Design, implementation, and test of variety and innovative solutions of ADCS.
- The setup of Hardware-In-the-Loop platforms for hardware and software validation.
- Writing design reviews and reports.

2019-2020: Assegno Di Ricerca Progetto "SIA-Italspazio-Implementation of an active magnetic control system for nanosatellites"

I kept working on my thesis project.

2016-2018: Master's thesis (Aerospace Engineering)

Helmholtz Cage calibration and Active Magnetic Control Design and Testing for CubeSat missions. This setup allows ADCS to be verified, using real on-board systems, evaluating their performance and indicating eventual design criticalities.
Tasks:

- Design and perform the coils and current driver board to produce the desired control action, within the constraints set on the time of operations, power consumption and electric current.
- Develop and implement of de-tumbling and a pointing control algorithm on FPGA.
- Setup and develop of Hardware in the loop, using System Generator, to verify the performance and robustness of the control algorithms and simulating critical scenarios.
- Implement PID control algorithm to drive the Helmholtz cage facility to accurately recreate the magnetic field along the spacecraft orbit.
- Calibrate and verify the magnetometer by using Least Square Method and Helmholtz cage facility.

2014-2015: Internship in HUAWEI Technologies
Study and planning of NGWDM 100G system on the network "Morocco Telecom" and coexistence between 10G and 100G systems.

2013: Internship in the National Telecommunications Regulatory Agency.
Setup of a network traffic monitoring tool and developing a web interface to provide real-time visibility into the network bandwidth performance.

2013: Didactic project (parking management system).

2012: Internship in the Ministry of Tourism (familiarizing with the working environment).

2011: Didactic project (automate lighting control system to reduce energy consumption).

PUBLICATIONS

Published Papers

M. Salim Farissi , Stefano Carletta , Augusto Nascetti and Paolo Teofilatto. Implementation and Hardware-In-The-Loop Simulation of a Magnetic Detumbling and Pointing Control Based on Three-Axis Magnetometer Data. Aerospace 2019, 6(12), 133, 11 December 2019.

Stefano Carletta , Paolo Teofilatto and M. Salim Farissi. A Magnetometer-Only Attitude Determination Strategy for Small Satellites: Design of the Algorithm and Hardware-in-the-Loop Testing. Aerospace 2020, 7(1), 3, 5 January 2020.

Conference Paper Presentations

2021: 72nd International Astronautical Congress (Status: Accepted and will be presented within 25 – 29 October 2021)

M. Salim Farissi, Ivan Agostinelli, Marco Mastrofini, Fabio Curti, Cosimo Marzo, Luigi Ansalone. Hardware implementation of the SPOT Payload for Orbiting Objects Detection using Star Sensors. 72nd International Astronautical Congress Dubai, United Arab Emirates 25 – 29 October 2021.

2019: 70th International Astronautical Congress 2019

M. Salim Farissi , Stefano Carletta , Augusto Nascetti and Paolo Teofilatto. Design And Hardware-In-The-Loop Test Of An Active Magnetic Detumbling And Pointing Control Based Only On Three-Axis Magnetometer Data. In Proceedings of the 70th International Astronautical Congress, Washington, D.C., 21–25 October 2019.

2020: 5th IAA Conference on University Satellite Missions and CubeSat Workshop

M. Salim Farissi , Stefano Carletta , Augusto Nascetti and Paolo Teofilatto. An Innovative Implementation of the TRIAD and EKF Algorithms on FPGA using Systolic Array Architecture for Real-Time Attitude Determination. 5th IAA Conference on University Satellite Missions and CubeSat Workshop, Rome ,Italy, January 28-31, 2020.

M. Salim Farissi , Stefano Carletta , Augusto Nascetti and Paolo Teofilatto. On-Board Computer Based on SRAM FPGA for PocketQube Missions. 5th IAA Conference on University Satellite Missions and CubeSat Workshop, Rome ,Italy, January 28-31, 2020.

SKILLS

Aerospace
ADCS, GNC, electronics for space systems, robotic systems, aerospace trajectories, Formation flying.
Electronics
SoC, FPGA, MCU, design and construction of PCB, embedded system, VLSI, communication peripherals (I^2C, SPI, UART, AXI MABA).
Telecommunications
Optical communication, source and channel coding, signal/image processing, radio frequency communication, SDR.
Programming Languages
VHDL, SystemVerilog (UVM), TCL, C/C++, Embedded C.
Software
Matlab, Simulink, System Generator, Vivado, HLS, SDK, ModelSim, WrightRapid, Altium, Code Composer Studio, Arduino, GNU Radio.
Others
Basics in project management, Concurrent Engineering and Mission Analysis.

PERSONAL CAPACITY

Sense of responsibility, work motivation and professionalism.
Good capacity for learning and applying new techniques.
Rigorous, punctual, tireless.
Autonomous and able to work in a multidisciplinary team.

LANGUAGES

Arabic & Tamazight: Fluent.
French & English: Good.
Italian: Basic.