EUROPEAN CURRICULUM VITAE FORMAT

PERSONAL INFORMATION

Name	**ANTONIO MASTRANDREA**
Telephone	
E-mail	
Nationality	

EXPERTISE

Design and implementation of digital hardware and firmware focused on system control and signal processing based on microcontrollers, ASIC/FPGAs, DSP.

WORK EXPERIENCE

• Dates (from – to)	7 April 2021 – 07 December 2021
Name and address of employer	Sapienza, University Of Rome – DIET
• Main activities and responsibilities	Sintesi e ottimizzazione RTL su FPGA e ASIC di acceleratori di calcolo riconfigurabili
• Dates (from – to)	1 April 2021 – 30 September 2021
Name and address of employer	Alma Mater Studiorum , University Of Bologna – DEI Guglielmo Marconi
• Main activities and responsibilities	Integrazione in Pulp Controller del nuovo protocollo MCTP per la comunicazione con il BMC.
• Dates (from – to)	8 June 2020 – 07 December 2020
Name and address of employer	Alma Mater Studiorum , University Of Bologna – DEI Guglielmo Marconi
• Main activities and responsibilities	Integrazione di PULP controller open-source con BMC e sensori ad alta frequenza di potenza
Dates (from – to)	1 June 2020 – 31 January 2021
Name and address of employer	Sapienza, University Of Rome – DIET
• Main activities and responsibilities	Progettazione di sottositema di debug per processori RISC-V
Dates (from – to)	23 May 2022 – 22 November 2022
Name and address of employer	Sapienza, University Of Rome – DIET
• Main activities and responsibilities	Sviluppo, prototipazione e testing di componenti per processori vettoriali
Dates (from – to)	6 October 2022 – 5 December 2022
Name and address of employer	Sapienza, University Of Rome – DIET
• Main activities and responsibilities	Sviluppo di circuiti elettronici miniaturizzati da inserire all'interno di una smart face mask
• Dates (from – to)	December 2018 – 30 November 2019
• Name and address of employer	Alma Mater Studiorum , University Of Bologna – DEI Guglielmo Marconi
• Type of business or sector	Electronic engineering
• Occupation or position held	Research Assistant
• Main activities and responsibilities	Design of a superscalar RISC-V processor for high-performance accelerators

Dates (from – to)	December 2018 – December 2021
Name and address of employer	Alma Mater Studiorum , University Of Bologna – DEI Guglielmo Marconi
Main activities and responsibilities	European Project: European Processor Initiative (EPI)- Power Management Subsystem
• Dates (from – to)	December 2013 – November 2018
• Name and address of employer	Sapienza, University Of Rome – DIET
• Type of business or sector	Electronic engineering
• Occupation or position held	Research Assistant
• Main activities and responsibilities	Probability of failure of digital cells in CMOS and FINFET technologies.
• Dates (from – to)	December 2016 – **Present**
• Name and address of employer	Sapienza, University Of Rome – DIET
• Type of business or sector	Electronic engineering
• Occupation or position held	Adjunct Professor (Professore a contratto)
• Main activities and responsibilities	Digital System Programming (Master's level course) .

EDUCATION AND TRAINING

• Dates	
• Name and type of organization providing education and training	Sapienza, University Of Rome – DIET
• Principal subjects/occupational skills covered	**PhD** research activity in Electronic Engineering
• Title of qualification awarded	Statistical characterization, analysis and modeling of speed performance in digital standard cell designs subject to process variations.
• Dates	
• Name and type of organization providing education and training	Sapienza, University Of Rome
• Principal subjects/occupational skills covered	**Master Degree (110/110 cum laude)**. (prof. Mauro Olivieri, DIET, Univ. Sapienza of Rome).
• Title of qualification awarded	"Sviluppo di modelli statistici di ritardo di celle standard in tecnologia nano-Cmos" Work Environment: HSPICE, NGSPICE
• Dates	
• Name and type of organisation providing education and training	Sapienza, University Of Rome
• Principal subjects/occupational skills covered	**Laurea Triennale in Ingegneria Elettronica (100/110)**: Low Power Cache Memory Design on STMicroelectronics. Prof. Ing. Mauro Olivieri – Sapienza, University Of Rome & Francesco Pappalardo – STMicroelectronics
• Dates	
• Name and type of organization providing education and training	Liceo Parmenide Roccadaspide (SA) – Scientific High School
• Title of qualification awarded	**Scientific High School Diploma (60/60)**

TECHNICAL SKILLS AND COMPETENCES

HARDWARE DESIGN

- Hardware description languages: VHDL, Verilog & SytemVerilog
- Mentor Modelsim & Questasim HDL simulation tools
- Altera Quartus Prime, MICROSEMI Libero IDE and Xilinx ISE & Vivado tools
- Synopsys Synplify Pro and Synplify ME FPGA/ASIC synthesis tools
- Synopsys Design Compiler (dc_shell)
- Microchip PIC and AVR microcontrollers, MPLABX IDE and XC compilers
- Cadence ORCAD 16.6/ Pspice HW simulation and design tool
- HSPICE, NGSPICE
- ALTIUM PCB Designer
- RS232, RS422, RS485, UART, SPI, I2C.
- Laboratory Instrumentation (Oscilloscope, Logic State Analyzer, Serial Protocol Analyzer)

SOFTWARE DESIGN

- C and C++ programming languages (GCC compiler)
- Yocto
- Assembly language (Microchip PIC12F,PIC16F,PIC18F,Atmega8)
- BASH, TCL & Python scripting languages
- UART, SPI, I2C, JTAG (read device registers and device programming), USB (CDC, HID & bulk).
- NVIDIA CUDA HW architecture and CUDA C programming language
- MATLAB computing environment (Signal Processing Toolbox, Control System Toolbox)
- UML & SysML.

OTHER CAPABILITIES

- Linux OS such as Ubuntu (12.04/14.04/16.04), Linux Mint (17/18)
- Windows OS (XP/7/8/8.1/10)
- Microsoft Office 2010/2016 suite
- Good PC assembly and repairing capability
- Good HDD data recovery capability using both Windows and DEFT/KALI Linux OS.
- Good practice in design and HW realization of electronics boards for audio and home control applications, such as modified guitar stomp boxes, stabilized power supply, home remote-control systems.

EXPERIENCES

SCHEMATIC DESIGN, PCB REALIZATION & SW PROGRAMMING:

- Microcontroller-based Boards (PIC12F,PIC16F,PIC18F,ATMEGA)
  - USB to Serial Converter
  - HID programmer (PIC family)
  - SPI & JTAG programmer (Atmega & FPGA)
  - HardDisk 16KB!
  - MIDI protocol sniffer
  - Streetlight expo 2015
  - Metal detector
- FPGA-based Boards with FPGA (SPARTAN3 and SPARTAN6)
  - development board with programmer

SW PROGRAMMING AND FPGA LOGIC SYNTHESIS

- Nexys3board (e.g: Arcade Pacman, z80)
- Nexys4 board (e.g.: ov7670)
- Zedboard
- Zybo board
- OZ745 Omnitek Zombie board
- Raspberry PI2, Pi3, Pi Zero W development boards, either with Linux OS support (Raspbian) or bare metal programming.
- YOCTO and openBmc on raspberry
- Arietta acmesystems board
- Nucleo ST + IKS01A1 board
- Pulpissimo with RISCV (Riscy) core on FPGA (debug with openOCD and gdb).
- Pulp-Controller on FPGA (debug with openOCD and gdb).
- Verilator testbench for RISCV core.
- Pulpino with RISCV core (Riscy and Klessydra) on FPGA.

PERSONAL SKILLS AND COMPETENCES

MOTHER TONGUE **Italian**

OTHER LANGUAGES

English

• *Reading skills*	Good
• *Writing skills*	Intermediate
• *Verbal skills*	Good (technical), intermediate (general)

Français

• *compétences en lecture*	Niveau
• *compétences en écriture*	Niveau
• *compétences à parler*	Niveau

SOCIAL SKILLS AND COMPETENCES

- Football Team experience during Elementary, Intermediate and High School (for 15 years).

ORGANISATIONAL SKILLS AND COMPETENCES

- Good Organizational Skills and Team-working competences gained during public event organization (e.g.: ISLPED 2015).

DRIVING LICENCE(S) European Driving License (B)

PUBLICATIONS

[1] Z Abbas, A Zahra, M Olivieri, A Mastrandrea, "Geometry Scaling Impact on Leakage Currents in FinFET Standard Cells Based on a Logic-Level Leakage Estimation Technique", Microelectronics, Electromagnetics and Telecommunications, 283-294, Springer, Singapore

[2] M Olivieri, U Khalid, A Mastrandrea, F Menichelli, "Characterizing noise pulse effects on the power consumption of idle digital cells", Circuits and Systems (ISCAS), 2018 IEEE International Symposium on, 1-5

[3] G. Stazi, F.Menichelli, A.Mastrandrea, andM. Olivieri, "Introducing approximate memory support in linux kernel," in Ph. D. Research in Microelectronics and Electronics (PRIME), 2017 13th Conference on, pp. 97–100, IEEE, 2017

[4] M. Olivieri, F. Menichelli, and A. Mastrandrea, "Optimal pipeline stage balancing in the presence of large isolated interconnect delay," Electronics Letters, vol. 53, no. 4, pp. 229–231, 2017

[5] M. Olivieri, A. Cheikh, G. Cerutti, A. Mastrandrea, and F. Menichelli, "Investigation on the optimal pipeline organization in risc-v multi-threaded soft processor cores," in CAS (NGCAS), 2017 New Generation of, pp. 45–48, IEEE, 2017

[6] F. Menichelli, G. Stazi, A. Mastrandrea, and M. Olivieri, "An emulator for approximate memory platforms based on qemu," in International Conference on Applications in Electronics Pervading Industry, Environment and Society, pp. 153–159, Springer, 2016

[7] U. Khalid, A.Mastrandrea, andM. Olivieri, "Effect of nbti/pbti aging and process variations on write failures in mosfet and finfet flip-flops,"Microelectronics Reliability, vol. 55, no. 12, pp. 2614–2626, 2015

[8] U. Khalid, A. Mastrandrea, Z. Abbas, and M. Olivieri, "Variability aware modeling of seu induced failure probability of logic circuit paths in static conditions," in Reliability, Infocom Technologies and Optimization (ICRITO)(Trends and Future Directions), 2015 4th International Conference on, pp. 1–4,IEEE, 2015

[9] Z. Abbas, A. Mastrandrea, and M. Olivieri, "A voltage-based leakage current calculation scheme and its application to nanoscale mosfet and finfet standard-cell designs," Very Large Scale Integration (VLSI) Systems, IEEE Transactions on (Volume:22 , Issue: 12), vol. 22, pp. 2549 – 2560, Dec. 2014. ISSN : 1063-8210

[10] A. MASTRANDREA, "Statistical characterization, analysis and modeling of speed performance in digital standard cell designs subject to process variations," 2014

[11] U. Khalid, A. Mastrandrea, and M. Olivieri, "Safe operation region characterization for quantifying the reliability of cmos logic affected by process variations," in Microelectronics and Electronics (PRIME), 2014 10th Conference on Ph. D. Research in, pp. 1–4, IEEE, 2014

[12] U. Khalid, A. Mastrandrea, and M. Olivieri, "Novel approaches to quantify failure probability due to process variations in nano-scale cmos logic," in Microelectronics Proceedings-MIEL 2014, 2014 29th International Conference on, pp. 371–374, IEEE, 2014

[13] U. Khalid, A. Mastrandrea, and M. Olivieri, "Combined impact of nbti aging and process variations on noise margins of flip-flops," in Digital System Design (DSD), 2014 17th Euromicro Conference on, pp. 488–495, IEEE, 2014

[14] Z. Abbas, A. Mastrandrea, and M. Menichelli, Antonio andOlivieri, SPICE Simulations of Digital VLSI Cells (Chapter 7). Springer. in press

[15] U. Khalid, A. Mastrandrea, and M. Olivieri, "Using safe operation regions to assess the error probability of logic circuits due to process variations," in Integrated Reliability Workshop Final Report (IRW), 2013 IEEE International, pp. 177–180, IEEE, 2013

[16] M. Olivieri and A. Mastrandrea, "Logic drivers: A propagation delay modeling paradigm for statistical simulation of standard cell designs," Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, vol. PP ISSUE: 99, july 10 2013. ISSN : 1063-8210

[17] M. Olivieri and A. Mastrandrea, "A general design methodology for synchronous early-completion prediction adders in nano-cmos dsp architectures," VLSI Design Hindawi Publishing Corporation, vol. 2013, p. 2, 2013

[18] M. Olivieri and A.Mastrandrea, "A new logic-level delay modeling paradigm for nano-cmos standard cells variation-aware simulation," 20 - 22 Giugno 2012

[19] M. Olivieri and A.Mastrandrea, "A new logic level delay modeling paradigm for nano-cmos standard cells variation-aware simulation," March 16 2012. Dresden, Germany

[20] A. Mastrandrea, F. Menichelli, and M. Olivieri, "A delay model allowing nano-cmos standard cells statistical simulation at the logic level," in Ph. D. Research inMicroelectronics and Electronics (PRIME), 2011 7th Conference on, pp. 217–220, IEEE,

2011
[21] M. Olivieri, F. Menichelli, M. A., F. Ramundo, and P. Nenzi, “Contributions in evaluating the statistical impact of technology variations on delay and power dissipation of logic cells,” in ECMI 2010, 16-th European Conference on Mathematics for Industry, July 26-30 2010. Wuppertal, Germany
[22] P. Nenzi, R. Larice, M. Mastrandrea, Antonio andOlivieri, S. Perticaroli, F. Ramundo, L. Sainte-Cluque, L. Trajkovic, and H. Vogt, “Ngspice: an open platform for modeling and simulation from device to board level,” 8 December 2010. California MOS-AK
[23] Andrea Bartolini, Davide Rossi, Antonio Mastrandrea, Christian Conficoni, Simone Benatti, Andrea Tilli, Luca Benini, "A PULP-based Parallel Power Controller for Future Exascale Systems", 2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS)
[24] Abdallah Cheikh, Stefano Sordillo, Antonio Mastrandrea, Francesco Menichelli, Mauro Olivieri,"Efficient Mathematical Accelerator Design Coupled with an Interleaved Multi-threading RISC-V Microprocessor", International Conference on Applications in Electronics Pervading Industry, Environment and Society, 529-539 Springer.
[25] GGiulia Stazi, Antonio Mastrandrea, Mauro Olivieri, Francesco Menichelli, "Quality Aware Selective ECC for Approximate DRAM", International Conference on Applications in Electronics Pervading Industry, Environment and Society, 109-116 Springer.
[26] Luigi Blasi, Francesco Vigli, Abdallah Cheikh, Antonio Mastrandrea, Francesco Menichelli, Mauro Olivieri, "A RISC-V Fault-Tolerant Microcontroller Core Architecture Based on a Hardware Thread Full/Partial Protection and a Thread-Controlled Watch-Dog Timer", International Conference on Applications in Electronics Pervading Industry, Environment and Society,505-511 Springer.
[27] Giulia Stazi, Antonio Mastrandrea, Mauro Olivieri, Francesco Menichelli,” Quality Aware Approximate Memory in RISC-V Linux Kernel”, 2019 15th Conference on Ph. D Research in Microelectronics and Electronics (PRIME), 177-180 IEEE.
[28] Giulia Stazi, Antonio Mastrandrea, Mauro Olivieri, Francesco Menichelli,”Full System Emulation of Approximate Memory Platforms with AppropinQuo”, Journal of Low Power Electronics, 30-39, American Scientific Publishers.
[29] Giulia Stazi, Antonio Mastrandrea, Mauro Olivieri, Francesco Menichelli, ”Appropinquo: A platform emulator for exploring the approximate memory design space”, 2018 New Generation of CAS (NGCAS), 66-69, IEEE.
[30] Giulia Stazi, Antonio Mastrandrea, Mauro Olivieri, Francesco Menichelli, “Approximate Memory Support for Linux Early Allocators in ARM Architectures”, International Conference on Applications in Electronics Pervading Industry, Environment and Society, 429-435, Springer.
[31] Giulia Stazi, Federica Silvestri, Antonio Mastrandrea, Mauro Olivieri, Francesco Menichelli, “Synthesis Time Reconfigurable Floating Point Unit for Transprecision Computing”, nternational Conference on Applications in Electronics Pervading Industry, Environment and Society, 261-267 Springer.
[32] Abdallah Cheikh, Gianmarco Cerutti, Antonio Mastrandrea, Francesco Menichelli, Mauro Olivieri, “The Microarchitecture of a Multi-threaded RISC-V Compliant Processing Core Family for IoT”, Applications in Electronics Pervading Industry, Environment and Society: APPLEPIES 2017, V.512 p89, Springer.
[33] Giulia Stazi, Lorenzo Adani, Antonio Mastrandrea, Mauro Olivieri, Francesco Menichelli, “Impact of approximate memory data allocation on a h. 264 software video encoder”, International Conference on High Performance Computing, 545-553 Springer.
[34] Mauro Olivieri, Usman Khalid, Antonio Mastrandrea, Francesco Menichelli. “Characterizing noise pulse effects on the power consumption of idle digital cells”, 2018 IEEE International Symposium on Circuits and Systems (ISCAS), 1-5 IEEE.
[35] Abdallah Cheikh, Gianmarco Cerutti, Antonio Mastrandrea, Francesco Menichelli, Mauro Olivieri,” The microarchitecture of a multi-threaded RISC-V compliant processing core family for IoT end-nodes”, International Conference on Applications in Electronics Pervading Industry, Environment and Society, 89-97 Springer.
[36] G Stazi, F Silvestri, A Mastrandrea, M Olivieri, F Menichelli,” Synthesis time reconfigurable floating point unit for transprecision computing”, 2018/9/26, 261-267, Springer, Cham, International Conference on Applications in Electronics Pervading Industry, Environment and Society.
[37] Marcello Barbirotta, Antonio Mastrandrea, Francesco Menichelli, Francesco Vigli, Luigi Blasi, Abdallah Cheikh, Stefano Sordillo, Fabio Di Gennaro, Mauro Olivieri,” Fault resilience analysis of a RISC-V microprocessor design through a dedicated UVM environment”, 2020 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT).

[38] Stefano Sordillo, Abdallah Cheikh, Antonio Mastrandrea, Francesco Menichelli, Mauro Olivieri,"Customizable Vector Acceleration in Extreme-Edge Computing: A RISC-V Software/Hardware Architecture Study on VGG-16 Implementation", Electronics Multidisciplinary Digital Publishing Institute, V.10, n. 4, p.518
[39] Abdallah Cheikh, Stefano Sordillo, Antonio Mastrandrea, Francesco Menichelli, Giuseppe Scotti, Mauro Olivieri, "Klessydra-T: Designing Vector Coprocessors for Multi-Threaded Edge-Computing Cores", IEEE Micro 2021.
[40] Marcello Barbirotta, Abdallah Cheikh, Antonio Mastrandrea, Francesco Menichelli, Mauro Olivieri, "A Fault Tolerant soft-core obtained from an Interleaved-Multi-Threading RISC-V microprocessor design", 2021 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT).
[41] M Barbirotta, A Cheikh, A Mastrandrea, F Menichelli, M Olivieri, "Analysis of a Fault Tolerant Edge-Computing Microarchitecture Exploiting Vector Acceleration", 2022 17th Conference on Ph. D Research in Microelectronics and Electronics.

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