europass Curriculum vitae

PERSONAL INFORMATION Riccardo Della Sala

Gender Male | Nationality Italian

WORK EXPERIENCE

Since March 2024 Part-Time Digital and Analog Designer

Radio Analog Micro Electronics SRL

As an external part-time collaborator with Radio Analog Micro Electronics SRL, I am involved in both digital and analog design activities including digital filtering, FPGA design, and micro-controller development. I have also been involved in several space-related design projects, focusing on components used for power supply and board control.

March 2022-September 2022 Part-Time Analog Designer

Radio Analog Micro Electronics SRL

As an external part-time collaborator with Radio Analog Micro Electronics SRL, I served as a consultant for ams OSRAM and Silicon Labs, supporting the development and design of analog circuits. My main responsibilities included designing operational transconductance amplifiers and comparators within the Cadence environment.

EDUCATION AND TRAINING

Since November 2023 Postdoctoral Research Fellow

“La Sapienza” University of Rome, Course in Information and Communication Technology (ICT)

My research centers on the design and development of cryptographic primitives tailored for hardware cryptography, including True Random Number Generators and Physical Unclonable Functions. Additionally, in the context of analog and digital design for biomedical applications, I specialize in designing ultra-low voltage and ultra-low power building blocks (OTAs, Filters, ADCs, and Comparators) for resource-constrained devices. This involves utilizing digital standard cells or inverter-based topologies.

2020 – 2023 PhD in Electronic Engineering: Summa Cum Laude

“La Sapienza” University of Rome, Course in Information and Communication Technology (ICT)

My PhD research was mainly focused on ultra-lightweight Cryptographic primitives, such as True Random Number Generators and Physical Unclonable Functions, for Resource Constrained Device such as FPGA and ASIC. Furthermore, in the context of analog design, I’m focused on Ultra Low Voltage and Ultra Low Power architectures for IoT interfaces, such as OTAs, Filters, LNAs, Comparators and Sense Amplifiers.

2019-2020 Master’s degree in Electronic Engineering: Summa Cum Laude

“La Sapienza” University of Rome, Course in Information and Communication Technology (ICT)

My Master's degree thesis was focused on Physical Unclonable Function, both from an analog and a digital perspective. In the context of the analog design, I was focused on Regulated Cascode Current Mirrors, deepening in highly robust interface with respect to PVT variations. With respect to digital design on FPGA, I get into detail of Ultra Compact and Lightweight architectures, focusing on the Xilinx's FPGA.

2017-2018 **Bachelor's Degree in Electronic Engineering: Summa Cum Laude**

"La Sapienza" University of Rome, Course in Information and Communication Technology (ICT)

My Bachelor's degree thesis was focused on 6th order Butterworth filter for Neural Recording Applications, the project of the filter was also published in [1].

PERSONAL SKILLS

Mother tongue: Italian

Other languages

	UNDERSTANDING		SPEAKING		WRITING
	Listening	Reading	Spoken interaction	Spoken production	
English	C1	C1	C1	C1	C1

Levels: A1 and A2: Basic user – B1 and B2: Independent user – C1 and C2: Proficient user
Common European Framework of Reference for Languages

Communication skills Excellent communication and interpersonal skills including respect, empathy and clarity acquired through years of private teaching of Physics, Mathematics, Electronics and Computer Science for University and High School students.

Organisational / managerial skills Good organizational and management skills acquired through years of sport accompanied by school studies and classical music. Determination, dynamism and resilience acquired through years of individual sports at a competitive level such as men's artistic gymnastics and modern pentathlon. Team spirit, adaptability and flexibility acquired through years of volleyball at a competitive level, playing up to the Serie D championships.

Job-related skills
– In-depth knowledge of Linux and Linux based operating systems including Ubuntu, Fedora, Red Hat, Arch-Linux, Debian, Chrome OS;
– Good knowledge of office programs such as Microsoft Office suites, OpenOffice, Libre Office;
– Excellent knowledge of LaTeX;
– Excellent knowledge of software tools for the design and analysis of electronic circuits such as the Orcad suite, Cadence, Modelsim, Vivado, Xilinx-ISE;
– Excellent programming skills with C, C ++, Bash, Python, TCL, Verilog, VHDL.

Research Awards and Recognitions
– The paper [5] entitled "0.3 V, Rail-to-Rail, Ultralow-Power, Non-Tailed, Body-Driven, Sub-Threshold Amplifier" has been selected among the top 20 cited papers in 2021 in the Section "Energy Science and Technology" of MDPI, link to the news: https://www.mdpi.com/about/announcements/5235.
– The paper [3] entitled "A 0.3 V, Rail-to-Rail, Ultralow-Power, Non-Tailed, Body-Driven, Sub-Threshold Amplifier" has resulted among the highly cited papers in Section "Energy Science and Technology" of Applied Sciences MDPI.
– The paper [23] won the gold leaf certificate (certificate for the top 10% papers) at the 18th International Conference on PhD Research in Microelectronics and Electronics (PRIME)

Research Funding and Grants
– In 2023, I received the "avvio alla ricerca - Tipo 2" funding as the principal investigator, for a total amount of €2,332.
– In 2023, I received an "assegno di ricerca di tipo A dipartimentale" through a public selection process, which funded one year of research.

Scopus Metrics As of January 4th, 2025, according to the Scopus database, I have 42 publications with a total of 436 citations and an h-index of 14.

– h-index : 14 (Scopus Database, January 4th, 2025)
– citations : 436 (Scopus Database, January 4th, 2025)
– papers : 42 (Scopus Database, January 4th, 2025)

PUBLICATIONS

[1] **Riccardo Della Sala**, Pietro Monsurrò, Giuseppe Scotti, and Alessandro Trifiletti. "Area-Efficient Low-Power Bandpass Gm-C Filter for Epileptic Seizure Detection in 130nm CMOS". In: *2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. IEEE, Nov. 2019, pp. 298–301. URL : https://ieeexplore.ieee.org/abstract/document/8964753 .

[2] Davide Bellizia, **Riccardo Della Sala**, and Giuseppe Scotti. "SC-DDPL as a Countermeasure against Static Power Side-Channel Attacks". In: *Cryptography* 5.3 (June 2021), p. 16. URL : https://www.mdpi.com/2410-387X/5/3/16 .

[3] Francesco Centurelli, **Riccardo Della Sala**, Pietro Monsurrò, Giuseppe Scotti, and Alessandro Trifiletti. "A 0.3 V Rail-to-Rail Ultra-Low-Power OTA with Improved Bandwidth and Slew Rate". In: *Journal of Low Power Electronics and Applications* 11.2 (Apr. 2021), p. 19. URL : https://www.mdpi.com/2079-9268/11/2/19 .

[4] Francesco Centurelli, **Riccardo Della Sala**, Pietro Monsurrò, Giuseppe Scotti, and Alessandro Trifiletti. "A Novel OTA Architecture Exploiting Current Gain Stages to Boost Bandwidth and Slew-Rate". In: *Electronics* 10.14 (July 2021), p. 1638. URL : https://www.mdpi.com/2079-9292/10/14/1638 .

[5] Francesco Centurelli, **Riccardo Della Sala**, Giuseppe Scotti, and Alessandro Trifiletti. "A 0.3 V, Rail-to-Rail, Ultralow-Power, Non-Tailed, Body-Driven, Sub-Threshold Amplifier". In: *Applied Sciences* 11.6 (Mar. 2021), p. 2528. URL : https://www.mdpi.com/2076-3417/11/6/2528 .

[6] **Riccardo Della Sala**, Davide Bellizia, and Giuseppe Scotti. "A Novel Ultra-Compact FPGA-Compatible TRNG Architecture Exploiting Latched Ring Oscillators". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 69.3 (Oct. 2021), pp. 1672–1676. URL : https://ieeexplore.ieee.org/abstract/document/9581292 .

[7] **Riccardo Della Sala**, Davide Bellizia, and Giuseppe Scotti. "A Novel Ultra-Compact FPGA PUF: The DD-PUF". In: *Cryptography* 5.3 (Sept. 2021), p. 23. URL : https://www.mdpi.com/2410-387X/5/3/23.

[8] Francesco Centurelli, **Riccardo Della Sala**, Pietro Monsurrò, Giuseppe Scotti, and Alessandro Trifiletti. "A Tree-Based Architecture for High-Performance Ultra-Low-Voltage Amplifiers". In: *Journal of Low Power Electronics and Applications* 12.1 (Feb. 2022), p. 12. URL : https://www.mdpi.com/2079-9268/12/1/12 .

[9] Francesco Centurelli, **Riccardo Della Sala**, Pietro Monsurró, Pasquale Tommasino, and Alessandro Trifiletti. "An Ultra-Low-Voltage class-AB OTA exploiting local CMFB and Body-to-Gate interface". In: *AEU - International Journal of Electronics and Communications* 145 (Feb. 2022), p. 154081. URL : https://www.sciencedirect.com/science/article/pii/S1434841121004787 .

[10] Francesco Centurelli, **Riccardo Della Sala**, and Giuseppe Scotti. "A Standard-Cell-Based CMFB for Fully Synthesizable OTAs". In: *Journal of Low Power Electronics and Applications* 12.2 (May 2022), p. 27. URL : https://www.mdpi.com/2079-9268/12/2/27.

[11] **Riccardo Della Sala**, Davide Bellizia, and Giuseppe Scotti. "A Lightweight FPGA Compatible Weak-PUF Primitive Based on XOR Gates". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 69.6 (Mar. 2022), pp. 2972–2976. URL : https://ieeexplore.ieee.org/abstract/document/9728744 .

[12] **Riccardo Della Sala**, Davide Bellizia, and Giuseppe Scotti. "High-Throughput FPGA-Compatible TRNG Architecture Exploiting Multistimuli Metastable Cells". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 69.12 (Aug. 2022), pp. 4886–4897. URL : https://ieeexplore.ieee.org/abstract/document/9868141 .

[13] **Riccardo Della Sala**, Francesco Centurelli, Pietro Monsurrò, and Giuseppe Scotti. "High-efficiency 0.3V OTA in CMOS 130nm technology using current mirrors with gain". In: *2022 17th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*. IEEE, June 2022, pp. 69–72. URL: https://ieeexplore.ieee.org/abstract/document/9816823.

[14] **Riccardo Della Sala**, Francesco Centurelli, Pietro Monsurrò, and Giuseppe Scotti. "Sub-μW Front-End Low Noise Amplifier for Neural Recording Applications". In: *2022 17th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*. IEEE, June 2022, pp. 305–308. URL: https://ieeexplore.ieee.org/abstract/document/981683.3

[15] **Riccardo Della Sala**, Francesco Centurelli, Pietro Monsurrò, Giuseppe Scotti, and Alessandro Trifiletti. "A body-driven rail-to-rail 0.3 V operational transconductance amplifier exploiting current gain stages". In: *International Journal of Circuit Theory and Applications* n/a.n/a (Dec. 2022). URL: https://doi.org/10.1002/cta.3520.

[16] **Riccardo Della Sala**, Francesco Centurelli, and Giuseppe Scotti. "A Novel Differential to Single-Ended Converter for Ultra-Low-Voltage Inverter-Based OTAs". In: *IEEE Access* 10 (Sept. 2022), pp. 98179–98190. URL: https://ieeexplore.ieee.org/abstract/document/9889717.

[17] **Riccardo Della Sala**, Francesco Centurelli, and Giuseppe Scotti. "Enabling ULV Fully Synthesizable Analog Circuits: The BA Cell, a Standard-Cell-Based Building Block for Analog Design". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 69.12 (Aug. 2022), pp. 4689–4693. URL: https://ieeexplore.ieee.org/abstract/document/985808.8

[18] **Riccardo Della Sala**, Francesco Centurelli, Giuseppe Scotti, Pasquale Tommasino, and Alessandro Trifiletti. "A Differential-to-Single-Ended Converter Based on Enhanced Body-Driven Current Mirrors Targeting Ultra-Low-Voltage OTAs". In: *Electronics* 11.23 (Nov. 2022), p. 3838. URL: https://www.mdpi.com/2079- 9292/11/23/3838.

[19] **Riccardo Della Sala** and Giuseppe Scotti. "The DD-Cell: a Double Side Entropic Source exploitable as PUF and TRNG". In: *2022 17th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*. IEEE, June 2022, pp. 353–356. URL: https://ieeexplore.ieee.org/abstract/document/9816824.

[20] Cristian Bocciarelli, Francesco Centurelli, **Riccardo Della Sala**, Valerio Spinogatti, and Alessandro Trifiletti. "A 2.5 GHz, 0.6 V Body Driven Dynamic Comparator Exploiting Charge Pump Based Dynamic Biasing". In: *2023 18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*. IEEE, 2023, pp. 18–21. URL: https://ieeexplore.ieee.org/abstract/document/10161910.

[21] **Riccardo Della Sala**, Davide Bellizia, Francesco Centurelli, and Giuseppe Scotti. "A Monostable Physically Unclonable Function Based on Improved RCCMs with 0–1.56% Native Bit Instability at 0.6–1.2 V and 0–75 °C". In: *Electronics* 12.3 (Feb. 2023), p. 755. URL: https://www.mdpi.com/2079-9292/12/3/755.

[22] **Riccardo Della Sala**, Davide Bellizia, Francesco Centurelli, Giuseppe Scotti, and Alessandro Trifiletti. "An Ultra Low Voltage Physical Unclonable Function Exploiting Body-Driven". In: *Proceedings of SIE 2023*. Cham, Switzerland: Springer, Nov. 2023, pp. 36–42.

[23] **Riccardo Della Sala**, Cristian Bocciarelli, Francesco Centurelli, Valerio Spinogatti, and Alessandro Trifiletti. "A Novel Ultra-Low Voltage Fully Synthesizable Comparator exploiting NAND Gates". In: *2023 18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*. IEEE, 2023, pp. 18–21.

[24] **Riccardo Della Sala**, Francesco Centurelli, Pietro Monsurrò, Giuseppe Scotti, and Alessandro Trifiletti. "A 0.3 V Three-Stage Body-Driven OTA". In: *Proceedings of SIE 2022*. Cham, Switzerland: Springer, Feb. 2023, pp. 21–26. URL: https://link.springer.com/chapter/10.1007/978-3-031-26066-7_4.

[25] **Riccardo Della Sala**, Francesco Centurelli, Pietro Monsurrò, Giuseppe Scotti, and Alessandro Trifiletti. "A 0.3V Rail-to-Rail Three-Stage OTA With High DC Gain and Improved Robustness to PVT Variations". In: *IEEE Access* 11 (Feb. 2023), pp. 19635–19644. URL : https://ieeexplore.ieee.org/abstract/document/10050798 .

[26] **Riccardo Della Sala**, Francesco Centurelli, and Giuseppe Scotti. "A High Performance 0.3 V Standard-Cell-Based OTA Suitable for Automatic Layout Flow". In: *Applied Sciences* 13.9 (Apr. 2023), p. 5517. URL : https://www.mdpi.com/2076-3417/13/9/5517.

[27] **Riccardo Della Sala**, Francesco Centurelli, Giuseppe Scotti, and Gaetano Palumbo. "Standard-Cell-Based Comparators for Ultra-Low Voltage Applications: Analysis and Comparisons". In: *Chips* 2.3 (Aug. 2023), pp. 173–194. URL : https://www.mdpi.com/2674-0729/2/3/11.

[28] **Riccardo Della Sala** and Giuseppe Scotti. "A Novel FPGA Implementation of the NAND-PUF with Minimal Resource Usage and High Reliability". In: *Cryptography* 7.2 (Apr. 2023), p. 18. URL : https://www.mdpi.com/2410-387X/7/2/18 .

[29] **Riccardo Della Sala** and Giuseppe Scotti. "Exploiting the DD-Cell as an Ultra-Compact Entropy Source for an FPGA-Based Re-Configurable PUF-TRNG Architecture". In: *IEEE Access* 11 (Aug. 2023), pp. 86178–86195. URL : https://ieeexplore.ieee.org/abstract/document/10216294 .

[30] **Riccardo Della Sala**, Valerio Spinogatti, Cristian Bocciarelli, Francesco Centurelli, and Alessandro Trifiletti. "A 0.15-to-0.5 V Body-Driven Dynamic Comparator with Rail-to-Rail ICMR". In: *Journal of Low Power Electronics and Applications* 13.2 (May 2023), p. 35. URL : https://www.mdpi.com/2079-9268/13/2/35 .

[31] Valerio Spinogatti, **Riccardo Della Sala**, Cristian Bocciarelli, Francesco Centurelli, and Alessandro Trifiletti. "An Improved Strong Arm Comparator With Integrated Static Preamplifier". In: *IEEE Access* 11 (Aug. 2023), pp. 91724–91737. URL : https://ieeexplore.ieee.org/abstract/document/10229118 .

[32] **Riccardo Della Sala**, Davide Bellizia, Francesco Centurelli, Giuseppe Scotti, and Alessandro Trifiletti. "Exploiting Body-Driven Feedbacks in Physical Unclonable Functions for Ultra Low Voltage, Ultra Low Power Applications: A 0.3 V Weak-PUF". In: *IEEE Trans. Circ. Syst. I* (May 2024), pp. 1–0.

[33] **Riccardo Della Sala**, Davide Bellizia, and Giuseppe Scotti. "Unveiling the True Power of the Latched Ring Oscillator for a Unified PUF and TRNG Architecture". In: *IEEE Trans. Very Large Scale Integr. VLSI Syst.* 32.12 (Sept. 2024), pp. 2403–2407.

[34] **Riccardo Della Sala**, Francesco Centurelli, Pietro Monsurró, and Giuseppe Scotti. "On the Feasibility of Cascode and Regulated Cascode Amplifier Stages in ULV Circuits Exploiting MOS Transistors in Deep Subthreshold Operation". In: *IEEE Access* 12 (2024), pp. 73292–73303.

[35] **Riccardo Della Sala**, Francesco Centurelli, and Giuseppe Scotti. "A Novel High Performance Standard-Cell Based ULV OTA Exploiting an Improved Basic Amplifier". In: *IEEE Access* 12 (Jan. 2024), pp. 17513–17521.

[36] **Riccardo Della Sala**, Francesco Centurelli, and Giuseppe Scotti. "A Novel Technique to Design Ultra-Low Voltage and Ultra-Low Power Inverter-Based OTAs". In: *2024 19th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*. 2024, pp. 1–4.

[37] **Riccardo Della Sala**, Francesco Centurelli, and Giuseppe Scotti. "An Ultra-Low-Voltage Approach to Accurately Set the Quiescent Current of Digital Standard Cells Used for Analog Design and Its Application on an Inverter-Based Operational Transconductance Amplifier". In: *J. Low Power Electron. Appl.* 14.3 (July 2024), p. 39.

[38] **Riccardo Della Sala**, Francesco Centurelli, and Giuseppe Scotti. "An Ultra-Low-Voltage Approach to Accurately Set the Quiescent Current of Digital Standard Cells Used for Analog Design and Its Application on an Inverter-Based Operational Transconductance Amplifier". In: *J. Low Power Electron. Appl.* 14.3 (July 2024), p. 39.

[39] **Riccardo Della Sala**, Francesco Centurelli, Giuseppe Scotti, and Gaetano Palumbo. "Rail to Rail ICMR and High Performance ULV Standard-Cell-Based Comparator for Biomedical and IoT Applications". In: *IEEE Access* (Jan. 2024), p. 1.

[40] **Riccardo Della Sala**, Francesco Centurelli, Giuseppe Scotti, and Alessandro Trifiletti. "A 0.3 V OTA with Enhanced CMRR and High Robustness to PVT Variations". In: *J. Low Power Electron. Appl.* 14.2 (Apr. 2024), p. 21.

[41] **Riccardo Della Sala** and Giuseppe Scotti. "On Enhancing the Throughput of the Latched Ring Oscillator TRNG on FPGA". In: *Applications in Electronics Pervading Industry, Environment and Society*. Cham, Switzerland: Springer, Jan. 2024, pp. 277–283.

[42] Valerio Spinogatti, **Riccardo Della Sala**, Cristian Bocciarelli, Francesco Centurelli, and Alessandro Trifiletti. "Body Biasing Techniques for Dynamic Comparators: A Systematic Survey". In: *Electronics* 13.4 (Feb. 2024), p. 711.

[43] **Riccardo Della Sala**, Cristian Bocciarelli, Valerio Spinogatti, Francesco Centurelli, and Alessandro Trifiletti. "Enhancing Performance of Ultra-Low Voltage Body-Driven Comparators Through Clocked Supply Voltage". In: *2024 19th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*. IEEE, pp. 09–12.

[44] **Riccardo Della Sala** and Giuseppe Scotti. "Evaluation and Comparison of Physical Unclonable Functions suitable for FPGA Implementation". In: *2024 39th Conference on Design of Circuits and Integrated Systems (DCIS)*. IEEE, pp. 13–15.

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