Pietro Monsurrò
Curriculum Vitae

Parte I – Informazioni generali

Nome e Cognome	Pietro Monsurrò
Lingue parlate	Italiano (madrelingua), Inglese (avanzato)

Parte II – Istruzione

Titolo	Anno	Università	Note
Laurea	2002	Università di Roma Sapienza	Ingegneria Elettronica
Laurea specialistica	2004	Università di Roma Sapienza	Ingegneria Elettronica
Dottorato di ricerca	2008	Università di Roma Sapienza	Ingegneria Elettronica
Diploma for Graduates	2009	University of London (UK)	Economics

Parte III – Incarichi

IIIA – Incarichi accademici

Inizio	Fine	Istituzione	Posizione
1/6/2005	30/9/2005	Università di Paderborn (Germania)	Ricercatore in visita
2/12/2013	31/3/2014	Università di Paderborn (Germania)	Ricercatore in visita

IIIB – Altri incarichi

Inizio	Fine	Istituzione	Posizione
11/10/2017	Oggi	Journal of Circuits, Systems, and Computers	Associate Editor

Parte IV – Esperienza didattica

IVA – Corsi universitari

Anno	Università	Corso
2008-2009	Università di Roma "Sapienza"	Laboratorio Interdisciplinare I, Corso di Laurea in Ingegneria Elettronica
2010-2011	Università di Roma "Sapienza", Sede di Latina	Elettronica II, 5 crediti, Corso di Laurea in Ingegneria dell'Informazione
2011-2012	Università di Roma "Sapienza", Sede di Latina	Elettronica II, 6 crediti, Corso di Laurea in Ingegneria dell'Informazione
2012-2013	Università di Roma "Sapienza", Sede di Latina	Elettronica II, 6 crediti, Corso di Laurea in Ingegneria dell'Informazione
2014-2015	Università di Roma "Sapienza", Sede di Latina	Elettronica II, 6 crediti, Corso di Laurea in Ingegneria dell'Informazione
2015-2016	Università di Roma "Sapienza", Sede di Sora (Ospedale)	Misure elettriche ed elettroniche, 1 credito, Corso di Laurea in Tecniche di radiologia medica, per immagini e radioterapia
2015-2016	Università di Roma "Sapienza", Sede di Latina	Elettronica II, 6 crediti, Corso di Laurea in Ingegneria dell'Informazione
2016-2017	Università di Roma "Sapienza", Sede di Latina	Elettronica II, 6 crediti, Corso di Laurea in Ingegneria dell'Informazione

2017-2018	Università di Roma “Sapienza”, Sede di Latina	Elettronica II, 3 crediti, Corso di Laurea in Ingegneria dell’Informazione
2018-2019	Università di Roma “Sapienza”, Sede di Latina	Misure Elettriche, 6 crediti, Corso di Laurea in Ingegneria dell’Informazione
2018-2019	Università di Roma “Sapienza”, Sede di Latina	Elettronica II, 6 crediti, Corso di Laurea in Ingegneria dell’Informazione
2019-2020	Università di Roma “Sapienza”, Sede di Latina	Misure Elettriche, 3 crediti, Corso di Laurea in Ingegneria dell’Informazione
2019-2020	Università di Roma “Sapienza”, Sede di Latina	Elettronica 2, 6 crediti, Corso di Laurea in Ingegneria dell’Informazione

IVB – Corsi di Dottorato

2018-2019	Università di Roma “Sapienza”	Digital calibration of analog, mixed-signal and Radio-Frequency systems, 2 crediti

Parte V – Attività di ricerca

Titolo	Descrizione breve
Time-interleaved ADCs	Modellizzazione e calibrazione di convertitori A/D paralleli
Low-voltage circuits	Circuiti integrati analogici e mixed-signal a bassa tensione di alimentazione
Low-power circuits	Circuiti integrati analogici e mixed-signal a basso consumo di potenza, inclusi circuiti in classe AB
Behavioural models	Modelli comportamentali lineari e nonlineari di sistemi analogici e mixed-signal

Parte VI – Indicatori bibliometrici

Tipo	Numero	Database	Inizio	Fine
Riviste internazionali	35	Scopus	2005	2020

Numero di citazioni	496
Hirsch (H) index	14

Parte VII – Abilitazione Scientifica Nazionale (ASN)

Abilitazione Scientifica Nazionale (ASN) ottenuta il 28/08/2018, Settore 09/E3, II Fascia, V Quadrimestre, Tornata 2016-2018, validità dal 28/08/2018 al 28/08/2024.

Parte VIII – Progetti di ricerca finanziati e attività di ricerca con aziende

VIIIA – Attività in progetti di ricerca finanziati

- SCARD, Side Channel Analysis Resistant Design Flow: STREP VI Programma quadro.
- SPREWS, Signal Processing for Radar and Electronic Warfare Systems: EDA Ad Hoc Type B Proposal
- TARANTO, TowARds Advanced bicmos NanoTechnology platforms for rf to thz applicatiOns: H2020 – RIA 2016
- GANIMEDE G4S, GANIMED 4 SIGINT - Sistema di analisi dello spettro radio a banda larga, POR FESR LAZIO 2014-2020, Avviso pubblico “Aerospazio e Sicurezza”

- ARDENT – sistema di beamforming in trasmissione in banda KA, POR FESR LAZIO 2014-2020, Avviso pubblico "KETS – Tecnologie abilitanti"
- Finanziamento ricerca di Ateneo: Piattaforme hardware riconfigurabili per lo studio e il dimensionamento di sistemi elettromeccanici per il controllo delle vibrazioni. Anno: 2005 (prot. C26A059871)
- Finanziamento per Progetti di Ricerca di Università: Architetture e topologie circuitali per sistemi microelettronici analogici e digitali ultra low voltage. Anno: 2007 (prot. C26A07BA5X)
- Finanziamento per Progetti di Ricerca di Università: Architetture e topologie circuitali per sistemi microelettronici analogici e digitali ultra low voltage. Anno: 2008 (prot. C26A08X7LS)
- Finanziamento per Progetti di Ricerca di Università: Sviluppo di convertitori analogico/digitali pipeline veloci a basso consumo di potenza per applicazioni biomediche. Anno: 2011 (prot. C26A11CSBN)

VIIIB – Attività di trasferimento tecnologico e consulenza verso aziende

- Oerlikon-Contraves (ora Rheinmetall), 2004: Sviluppo ASIC mixed signal per trattamento di segnale (fase prima).
- Oerlikon-Contraves (ora Rheinmetall), 2004: Sviluppo ASIC mixed signal per trattamento di segnale (fase seconda).
- Oerlikon-Contraves (ora Rheinmetall), 2005: Sviluppo ASIC mixed signal per trattamento di segnale (fase terza).
- Oerlikon-Contraves (ora Rheinmetall), 2007: Sviluppo ASIC mixed signal per trattamento di segnale (fase quarta).
- Oerlikon-Contraves (ora Rheinmetall), 2007: Sviluppo ASIC mixed signal per trattamento di segnale (fase quinta).
- Elettronica S.P.A., 2005: Studio di fattibilità di ricevitori digitali per l'analisi e la detezione di forme d'onda LPI.
- Elettronica S.P.A., 2007: Rivisitazione del progetto dell'ASIC GAM01: definizione ed applicazione modifiche per esecuzione terzo run.
- Elettronica S.P.A., 2008: Studio per la realizzazione di un ASIC (application specific integrated circuit).
- Elettronica S.p.A., 2010. "Esamina del progetto dell'ASIC GAM02 e individuazione delle marginalità/difetti"
- Tecnotiberis-Elmacom, 2006: "Sviluppo di moduli TX-RX per sistemi ESM"
- Thales Alenia Spazio Italia, 2009: Studio e modellistica di catene di amplificazione RF a larga banda, basso rumore ed elevata linearità per applicazioni in ambiente spaziale.
- Thales Alenia Spazio Italia, 2011: Sviluppo di simulatori digitali di filtri analogici a microonde.
- Thales Alenia Spazio Italia, 2012: Procurement of Wideband Link Emulator – Satellite Multi Channel & Repeater Emulator.
- Thales Alenia Spazio Italia, 2012: Procurement of Front-End for Wideband Link Emulator (WLE RF Interfaces &MMI)
- Space Engineering S.P.A., 2010: Supporto tecnico alle attività per la realizzazione di un MMIC per BFN per applicazioni spaziali.
- Space Engineering S.p.A., 2012: "Realizzazione di librerie AD e DA, di software di sviluppo e l'acquisto dei servizi di costruzione presso la fonderia"
- Interconsulting, 2011: Analisi Algoritmi e Finalizzazione.
- SELEX ELSAG, 2011: "Algoritmi di Direction Finding e forme d'onda intelligenti"
- DSO National Laboratories (Singapore), 2012: "Overall process workflow associated with the Radio-Frequency (RF) design and modelling of high speed Lithium Niobate modulator and photodiodes"
- Nanyang Technological University NTU (Singapore), 2016: Photonics consultancy for analysis and evaluation of a photonic 10-ENOB ADC system (both single-channel and multi-channel) with input bandwidth between 100MHz to 40GHz.
- Thales Alenia Spazio Italia, 2019: FOSTER – Flexible On-board Space Technologies for nExt geneRation multi-mission digital payloads

Parte IX – Partecipazione a conferenze e in comitati editoriali

IXA – Partecipazione in comitati editoriali di conferenze

Membro del Program Committee della 2017 European Conference on Circuit Theory and Design (ECCTD), tenutasi a Catania, Italia.

IXB – Partecipazioni a conferenze

1. 2005 IEEE International Symposium on Circuits and Systems (ISCAS), Kobe, Japan, 23-26/5/2005, paper: "High-speed CMOS-to-ECL pad driver in 0.18μm CMOS"
2. 2008 IEEE International Symposium on Circuits and Systems (ISCAS), Seattle, United States, 18-21/5/2008, paper: "A gain-enhancing technique for very low-voltage amplifiers"
3. 2011 European Conference on Circuit Theory and Design (ECCTD), Linkoping, Sweden, 29-31/8/2011, papers: "A class-AB flipped voltage follower output stage", "A class-AB very low voltage amplifier and sample & hold circuit", "An MDAC architecture with low sensitivity to finite opamp gain", "Design strategy for biquad-based continuous-time low-pass filters", "A very low-voltage differential amplifier for opamp design"
4. 2011 IMEKO TC4 International Workshop on ADC Modelling, Testing and Data Converter Analysis and Design, Orvieto, Italia, 30/6-1/7/2011, paper: "Digital background calibration of subsampling time-interleaved ADCs"
5. [2013 European Conference on Circuit Theory and Design (ECCTD), Dresda, Germania, 8-12/9/2013, paper: "Effect of components relative tolerance in the magnitude response of a Gm-C biquad"
6. 2014 International Conference on Mixed Design of Integrated Circuits and Systems, 19-21/6/2014, Lublin, Poland, papers: "Implementing radar algorithms on CUDA hardware", "Architecture and modeling of a novel optical beamforming network suitable for microwave photonics implementation"
7. 2014 Astronomical Telescopes + Instrumentation, SPIE - The International Society for Optical Engineering, Montreal, Canada, 22-27/6/2014, paper: "Using feed array networks to control distortions in antenna reflector for astrophysical radio-astronomy"
8. 2016 23st International Conference on Mixed Design of Integrated Circuits and Systems, Lodz, Poland, 23-25/6/2016, papers: "A new class-AB Flipped Voltage Follower using a common-gate auxiliary amplifier", "Synthesis of anti-aliasing filters for IF receivers"
9. 2016 Astronomical Telescopes + Instrumentation, SPIE - The International Society for Optical Engineering, Edinburg, UK, 10-15/6/2016, papers: "Design-oriented analytic model of phase and frequency modulated optical links", "Blind and reference channel-based time interleaved ADC calibration schemes: A comparison", "AM-AM/AM-PM distortion versus complex Volterra kernels for modeling RF transceiver blocks"
10. 2017 European Conference on Circuit Theory and Design (ECCTD), Catania, Italia, 4-6/9/2017, papers: "The recursive batch least squares filter: An efficient RLS filter for floating-point hardware", "VHDL implementation of FWL RLS algorithm", "Perfect reconstruction filters for 4-channels time-interleaved ADC affected by mismatches", "On the use of voltage conveyors for the synthesis of biquad filters and arbitrary networks", "A fully-differential class-AB OTA with CMRR improved by local feedback", "Class-AB current conveyors based on the FVF", "Power-efficient dynamic-biased CCII"
11. 2017 IEEE International Instrumentation and Measurement Technology Conference (I2MTC), Torino, Italia, 22-25/5/2017, paper: "Multi-rate signal processing based model for high-speed digitizers"
12. 2018 IMEKO World Congress, Belfast, UK, 3-6/9/2018, papers: "A 2-channel digitizer based on MFP strategy", "Parallel and hierarchical architectures of 4-channel MFP digitizer".

Parte X – Lista completa delle pubblicazioni a rivista e a conferenza

XA – Pubblicazioni su riviste internazionali

1. Centurelli, F., Monsurrò, P., Scotti, G., Tommasino, P., Trifiletti, A., "10-ghz fully differential sallen–key lowpass biquad filters in 55nm sige BICMOS technology", (2020) Electronics (Switzerland), 9 (4), art. no. 563.
2. Centurelli, F., Monsurrò, P., Stornelli, V., Barile, G., Trifiletti, A., "Low-power class-AB 4th-order low-pass filter based on current conveyors with dynamic mismatch compensation of biasing errors", (2020) International Journal of Circuit Theory and Applications, 48 (4), pp. 472-484.

3. Cellucci, D., Centurelli, F., Di Stefano, V., Monsurrò, P., Pennisi, S., Scotti, G., Trifiletti, A., “0.6-V CMOS cascode OTA with complementary gate-driven gain-boosting and forward body bias”, (2020) International Journal of Circuit Theory and Applications, 48 (1), pp. 15-27.
4. Monsurrò, P., Trifiletti, A., Angrisani, L., D'Arco, M., “Two novel architectures for 4-channel mixing/filtering/processing digitizers”, (2019) Measurement: Journal of the International Measurement Confederation, 142, pp. 138-147.
5. Centurelli, F., Monsurrò, P., Trifiletti, A., “High-gain, high-CMRR class AB operational transconductance amplifier based on the flipped voltage follower”, (2019) International Journal of Circuit Theory and Applications, 47 (4), pp. 499-512.
6. Centurelli, F., Monsurrò, P., Parisi, G., Tommasino, P., Trifiletti, A., “A Topology of Fully Differential Class-AB Symmetrical OTA with Improved CMRR”, (2018) IEEE Transactions on Circuits and Systems II: Express Briefs, 65 (11), art. no. 8013759, pp. 1504-1508.
7. Monsurrò, P., Trifiletti, A., Angrisani, L., D'Arco, M., “Streamline calibration modelling for a comprehensive design of ATI-based digitizers”, (2018) Measurement: Journal of the International Measurement Confederation, 125, pp. 386-393.
8. Avoli, M., Centurelli, F., Monsurrò, P., Scotti, G., Trifiletti, A., “Low power DDA-based instrumentation amplifier for neural recording applications in 65 nm CMOS”, (2018) AEU - International Journal of Electronics and Communications, 92, pp. 30-35.
9. Centurelli, F., Monsurrò, P., Parisi, G., Tommasino, P., Trifiletti, A., “A 0.6 V class-AB rail-to-rail CMOS OTA exploiting threshold lowering”, (2018) Electronics Letters, 54 (15), pp. 930-932.
10. Bellizia, D., Bongiovanni, S., Monsurrò, P., Scotti, G., Trifiletti, A., Trotta, F.B., “Secure Double Rate Registers as an RTL Countermeasure Against Power Analysis Attacks”, (2018) IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 26 (7), pp. 1368-1376.
11. Monsurrò, P., Tommasino, P., Trifiletti, A., Vannucci, A., “Design of broadband high dynamic-range fiber optic links”, (2018) Journal of Optical Communications, 39 (2), pp. 185-190.
12. Monsurrò, P., Rosato, F., Trifiletti, A., “New Models for the Calibration of Four-Channel Time-Interleaved ADCs Using Filter Banks”, (2018) IEEE Transactions on Circuits and Systems II: Express Briefs, 65 (2), art. no. 7839278, pp. 141-145.
13. Centurelli, F., Monsurrò, P., Trifiletti, A., “A 10 GHz inductorless active SiGe HBT lowpass filter”, (2018) International Journal of RF and Microwave Computer-Aided Engineering, 28 (9), art. no. e21567.
14. Centurelli, F., Monsurrò, P., Parisi, G., Tommasino, P., Trifiletti, A., “Fully Differential Class-AB OTA with Improved CMRR”, (2017) Journal of Circuits, Systems and Computers, 26 (11), art. no. 1750169.
15. Stornelli, V., Pantoli, L., Ferri, G., Liberati, L., Centurelli, F., Monsurrò, P., Trifiletti, A., “The AB-CCII, a novel adaptive biasing LV-LP current conveyor architecture”, (2017) AEU - International Journal of Electronics and Communications, 79, pp. 301-306.
16. Bellizia, D., Bongiovanni, S., Monsurrò, P., Scotti, G., Trifiletti, A., “Univariate power analysis attacks exploiting static dissipation of nanometer CMOS VLSI circuits for cryptographic applications”, (2017) IEEE Transactions on Emerging Topics in Computing, 5 (3), art. no. 7465800, pp. 329-339.
17. Monsurrò, P., Trifiletti, A., “Calibration of Time-Interleaved ADCs via Hermitianity-Preserving Taylor Approximations”, (2017) IEEE Transactions on Circuits and Systems II: Express Briefs, 64 (4), art. no. 7464300, pp. 357-361.
18. Monsurrò, P., Trifiletti, A., “Faster, Stabler, and Simpler - A Recursive-Least-Squares Algorithm Exploiting the Frisch-Waugh-Lovell Theorem”, (2017) IEEE Transactions on Circuits and Systems II: Express Briefs, 64 (3), art. no. 7467509, pp. 344-348.
19. Centurelli, F., Monsurrò, P., Rosato, F., Ruscio, D., Trifiletti, A., “Calibration of pipeline ADC with pruned Volterra kernels”, (2016) Electronics Letters, 52 (16), pp. 1370-1371.
20. Centurelli, F., Monsurrò, P., Trifiletti, A., “Comparative performance analysis and complementary triode based CMFB circuits for fully differential class AB symmetrical OTAs with low power consumption”, (2016) International Journal of Circuit Theory and Applications, 44 (5), pp. 1039-1054.
21. Centurelli, F., Monsurrò, P., Rosato, F., Ruscio, D., Trifiletti, A., “Calibrating sample and hold stages with pruned Volterra kernels”, (2015) Electronics Letters, 51 (25), pp. 2094-2096.

22. Monsurrò, P., Trifiletti, A., “Subsampling Models of Bandwidth Mismatch for Time-Interleaved Converter Calibration”, (2015) IEEE Transactions on Circuits and Systems II: Express Briefs, 62 (10), art. no. 7163308, pp. 957-961.
23. Monsurrò, P., Pennisi, S., Scotti, G., Trifiletti, A., “High-tuning-range CMOS band-pass if filter based on a low-Q cascaded biquad optimization technique”, (2015) International Journal of Circuit Theory and Applications, 43 (11), pp. 1615-1636.
24. Scotti, G., Pennisi, S., Monsurrò, P., Trifiletti, A., “88-μ A 1-MHz stray-insensitive CMOS current-mode interface IC for differential capacitive sensors”, (2014) IEEE Transactions on Circuits and Systems I: Regular Papers, 61 (7), art. no. 6722992, pp. 1905-1916.
25. Centurelli, F., Monsurrò, P., Trifiletti, A., “Improved digital background calibration of time-interleaved pipeline A/D converters” (2013) IEEE Transactions on Circuits and Systems II: Express Briefs, 60 (2), art. no. 6476650, pp. 86-90.
26. Centurelli, F., Monsurrò, P., Trifiletti, A., “Efficient digital background calibration of time-interleaved pipeline analog-to-digital converters”, (2012) IEEE Transactions on Circuits and Systems I: Regular Papers, 59 (7), art. no. 6133305, pp. 1373-1383.
27. Monsurró, P., Pennisi, S., Scotti, G., Trifiletti, A., “Exploiting the body of MOS devices for high performance analog design”, (2011) IEEE Circuits and Systems Magazine, 11 (4), art. no. 6035851, pp. 8-23.
28. Centurelli, F., Monsurrò, P., Trifiletti, A., “Behavioral modeling for calibration of pipeline analog-to-digital converters”, (2010) IEEE Transactions on Circuits and Systems I: Regular Papers, 57 (6), art. no. 5395691, pp. 1255-1264.
29. Centurelli, F., Monsurrò, P., Pennisi, S., Scotti, G., Trifiletti, A., “Design solutions for sample-and-hold circuits in CMOS nanometer technologies”, (2009) IEEE Transactions on Circuits and Systems II: Express Briefs, 56 (6), pp. 459-463.
30. Grasso, A.D., Monsurrò, P., Pennisi, S., Scotti, G., Trifiletti, A., “Analysis and implementation of a minimum-supply body-biased CMOS differential amplifier cell”, (2009) IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 17 (2), pp. 172-180.
31. Monsurrò, P., Pennisi, S., Scotti, G., Trifiletti, A., “0.9-V CMOS cascode amplifier with body-driven gain boosting”, (2009) International Journal of Circuit Theory and Applications, 37 (2), pp. 193-202.
32. Monsurrò, P., Pennisi, S., Scotti, G., Trifiletti, A., “Unity-gain amplifier with theoretically zero gain error”, (2008) IEEE Transactions on Instrumentation and Measurement, 57 (7), pp. 1431-1437.
33. Centurelli, F., Monsurrò, P., Trifiletti, A., “A simple technique for fast digital background calibration of A/D converters”, (2008) Eurasip Journal on Advances in Signal Processing, 2008, art. no. 453218.
34. Monsurrò, P., Pennisi, S., Scotti, G., Trifiletti, A., “Linearization Technique for Source-Degenerated CMOS Differential Transconductors”, (2007) IEEE Transactions on Circuits and Systems II: Express Briefs, 54 (10), pp. 848-852.
35. Monsurrò, P., Scotti, G., Trifiletti, A., Pennisi, S., “Biasing technique via bulk terminal for minimum supply CMOS amplifiers”, (2005) Electronics Letters, 41 (14), pp. 779-780.
36. Centurelli, F., Monsurrò, P., Scotti, G., Tommasino, P., Trifiletti, A., “An improved reversed miller compensation technique for three-stage CMOS OTAs with double pole-zero cancellation and almost single-pole frequency”, (2020) International Journal of Circuit Theory and Applications (accepted, to be published).

XB – Pubblicazioni su conferenze internazionali

1. Angrisani, A., D'Arco, M., Monsurrò, P., Trifiletti, A.; Parallel and hierarchical architectures of 4-channel MFP digitizer; (2018) Journal of Physics: Conference Series, 1065 (5), art. no. 052003.
2. Angrisani, A., D'Arco, M., Monsurrò, P., Trifiletti, A.; A 2-channel digitizer based on MFP strategy; (2018) Journal of Physics: Conference Series, 1065 (5), art. no. 052002.
3. Manna, M.L., Monsurrò, P., Tommasino, P., Trifiletti, A.; Machine learning techniques for frequency sharing in a cognitive radar; (2018) 2018 IEEE Radar Conference, RadarConf 2018, pp. 732-735.
4. Lulli, G., Monsurrò, P., Rosato, F., Tomasicchio, G., Tommasino, P., Trifiletti, A.; Wideband nonlinearities correction in digital payloads channels with parallel architectures; (2018) IET Conference Publications, 2018 (CP752).

5. Monsurrò, P., Trifiletti, A.; The recursive batch least squares filter: An efficient RLS filter for floating-point hardware; (2017) 2017 European Conference on Circuit Theory and Design, ECCTD 2017, art. no. 8093223, .
6. Bellizia, D., Monsurrò, P., Trifiletti, A.; VHDL implementation of FWL RLS algorithm; (2017) 2017 European Conference on Circuit Theory and Design, ECCTD 2017, art. no. 8093356.
7. Rosato, F., Monsurrò, P., Trifiletti, A.; Perfect reconstruction filters for 4-channels time-interleaved ADC affected by mismatches; (2017) 2017 European Conference on Circuit Theory and Design, ECCTD 2017, art. no. 8093227.
8. Centurelli, F., Monsurrò, P., Tommasino, P., Trifiletti, A.; On the use of voltage conveyors for the synthesis of biquad filters and arbitrary networks; (2017) 2017 European Conference on Circuit Theory and Design, ECCTD 2017, art. no. 8093353.
9. Centurelli, F., Monsurrò, P., Parisi, G., Tommasino, P., Trifiletti, A.; A fully-differential class-AB OTA with CMRR improved by local feedback; (2017) 2017 European Conference on Circuit Theory and Design, ECCTD 2017, art. no. 8093355.
10. Centurelli, F., Monsurrò, P., Trifiletti, A., Barile, G., Ferri, G., Pantoli, L., Stornelli, V.; Class-AB current conveyors based on the FVF; (2017) 2017 European Conference on Circuit Theory and Design, ECCTD 2017, art. no. 8093354.
11. Barile, G., Liberati, L., Ferri, G., Pantoli, L., Stornelli, V., Centurelli, F., Monsurrò, P., Trifiletti, A.; Power-efficient dynamic-biased CCII; (2017) 2017 European Conference on Circuit Theory and Design, ECCTD 2017, art. no. 8093349.
12. Ruscio, D., Centurelli, F., Monsurrò, P., Trifiletti, A.; Reconfigurable low voltage inverter-based sample-and-hold amplifier; (2017) PRIME 2017 - 13th Conference on PhD Research in Microelectronics and Electronics, Proceedings, art. no. 7974125, pp. 133-136.
13. Monsurrò, P., Trifiletti, A., Angrisani, L., D'Arco, M.; Multi-rate signal processing based model for high-speed digitizers; (2017) I2MTC 2017 - 2017 IEEE International Instrumentation and Measurement Technology Conference, Proceedings, art. no. 7969823.
14. Lamanna, M., Monsurrò, P., Scotti, G., Tommasino, P., Trifiletti, A.; Spectrum estimation by multiple asynchronous channels; (2017) European Microwave Week 2017: "A Prime Year for a Prime Event", EuMW 2017 - Conference Proceedings; 14th European Microwave Conference, EURAD 2017, 2018-January, pp. 171-174.
15. Tomasicchio, G., Lulli, G., Monsurrò, P., Rosato, F., Tommasino, P., Trifiletti, A.; Models for wideband nonlinearities in satcom payloads receiver channels and their parallelism; (2017) Ka and Broadband Communications Conference, 2017-October.
16. Monsurrò, P., Trifiletti, A.; Synthesis of anti-aliasing filters for if receivers; (2016) Proceedings of the 23rd International Conference Mixed Design of Integrated Circuits and Systems, MIXDES 2016, art. no. 7529739, pp. 239-242.
17. Centurelli, F., Monsurrò, P., Ruscio, D., Trifiletti, A.; A new class-AB Flipped Voltage Follower using a common-gate auxiliary amplifier; (2016) Proceedings of the 23rd International Conference Mixed Design of Integrated Circuits and Systems, MIXDES 2016, art. no. 7529719, pp. 143-146.
18. La Manna, M., Monsurrò, P., Tommasino, P., Trifiletti, A.; Adaptive spectrum controlled waveforms for cognitive radar; (2016) 2016 IEEE Radar Conference, RadarConf 2016, art. no. 7485120.
19. Cimmino, R.F., Monsurrò, P., Romano, F., Scotti, G., Trifiletti, A.; AM-AM/AM-PM distortion versus complex Volterra kernels for modeling RF transceiver blocks; (2016) Proceedings of SPIE - The International Society for Optical Engineering, 9906, art. no. 99065Z.
20. Cimmino, R.F., Centurelli, F., Monsurrò, P., Romano, F., Trifiletti, A.; Blind and reference channel-based time interleaved ADC calibration schemes: A comparison; (2016) Proceedings of SPIE - The International Society for Optical Engineering, 9906, art. no. 990631.
21. Monsurrò, P., Saitto, A., Tommasino, P., Trifiletti, A., Vannucci, A., Cimmino, R.F.; Design-oriented analytic model of phase and frequency modulated optical links; (2016) Proceedings of SPIE - The International Society for Optical Engineering, 9904, art. no. 99045S.
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