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PERSONAL INFORMATION

Riccardo Della Sala

WORK EXPERIENCE

Since March 2025

Contract Professor of "Elettronica Digitale"

“La Sapienza” University of Rome, Course in Information and Communication Technology (ICT)

Since March 2025 – Teaching assignment (Elettronica Digitale, SSD IINF-01/A) at Sapienza University of Rome, Bachelor Degree in Information Engineering (Latina campus), under call IITO 3/2024, provision no. 439/2024.

Since March 2024

Part-Time Digital and Analog Designer

Radio Analog Micro Electronics SRL

As an external part-time collaborator with Radio Analog Micro Electronics SRL, I am involved in both digital and analog design activities including digital filtering, FPGA design, and microcontroller development. I have also been involved in several space-related design projects, focusing on components used for power supply and board control.

March 2022-September 2022

Part-Time Analog Designer

Radio Analog Micro Electronics SRL

As an external part-time collaborator with Radio Analog Micro Electronics SRL, I served as a consultant for ams OSRAM and Silicon Labs, supporting the development and design of analog circuits. My main responsibilities included designing operational transconductance amplifiers and comparators within the Cadence environment.

ACADEMIC APPOINTMENTS

1th November 2024 - 1th November 2025

Research fellow at the Department of Information Engineering, Electronics and Telecommunications of Sapienza University of Rome

1th November 2023 - 1th November 2024

Research fellow at the Department of Information Engineering, Electronics and Telecommunications of Sapienza University of Rome

TEACHING EXPERIENCE

26th September - 4th October 2024

“Ultra Low Voltage and Ultra Low Power Circuits for Biomedical and IoT Applications” Course

I was Professor of the course “Ultra Low Voltage and Ultra Low Power Circuits for Biomedical and IoT Applications”, held from September 26, 2024, to October 4, 2024, for a total of 15 teaching hours (equivalent to 5 ECTS credits, in accordance with the internal regulations of the PhD program in Science and Technology for Electronic and Telecommunication Engineering – STIET) at the Department of Naval, Electrical, Electronic and Telecommunications Engineering (DITEN) of the University of Genoa (UniGe).

25th September - 4th October 2024

"Physical Unclonable Functions and True Random Number Generators for Hardware Security and Cryptography" Course

I was the instructor of the PhD-level course "Physical Unclonable Functions and True Random Number Generators for Hardware Security and Cryptography", held from September 25, 2024, to October 4, 2024, for a total of 12 teaching hours (equivalent to 4 ECTS credits, in accordance with the internal regulations of the PhD program in *Science and Technology for Electronic and Telecommunication Engineering* – STIET) at the Department of Naval, Electrical, Electronic and Telecommunications Engineering (DITEN) of the University of Genoa (UniGe).

Second Semester of the Academic Year 2024/2025

"Digital Electronic" Course

I was the professor of the course "Digital Electronics", Scientific-Disciplinary Sector IINF-01/A (formerly ING-INF/01), for a total of 6 ECTS credits (in accordance with Sapienza's regulations), delivered during the second semester of the 2024/2025 academic year within the single-cycle Master's Degree Program in Information Engineering (Latina campus). The teaching assignment was identified by code 6 and announced by the Department of Computer, Control, and Management Engineering "A. Ruberti" under provision no. 439/2024, published on December 23, 2024, on the University's website, as part of call IITO 3/2024.

EDUCATION AND TRAINING

Since 13th March 2025

National Scientific qualification as associate professor in the Italian higher education system, in the call 2023/2025 (Ministerial Decree n. 1796/2023) for the disciplinary field of 09/E3 - Electronics.

ENG: National Scientific qualification as associate professor in the Italian higher education system, in the call 2023/2025 (Ministerial Decree n. 1796/2023) for the disciplinary field of 09/E3 - Electronics. (Academic Recruitment Field 09/E - Electrical and electronic engineering and measurements, according to the national classification). ITA: Abilitazione Scientifica Nazionale alle funzioni di professore universitario di seconda fascia nel Settore Concorsuale 09/E3 - ELETTRONICA, conseguita all'esito delle procedure bandite con Decreto Direttoriale n. DD 1796/2023.

Since November 2023

Postdoctoral Research Fellow

"La Sapienza" University of Rome, Course in Information and Communication Technology (ICT)

My research centers on the design and development of cryptographic primitives tailored for hardware cryptography, including True Random Number Generators and Physical Unclonable Functions. Additionally, in the context of analog and digital design for biomedical applications, I specialize in designing ultra-low voltage and ultra-low power building blocks (OTAs, Filters, ADCs, and Comparators) for resource-constrained devices. This involves utilizing digital standard cells or inverter-based topologies.

2020 – 2023

PhD in Electronic Engineering: Summa Cum Laude

"La Sapienza" University of Rome, Course in Information and Communication Technology (ICT)

My PhD research was mainly focused on ultra-lightweight Cryptographic primitives, such as True Random Number Generators and Physical Unclonable Functions, for Resource Constrained Device such as FPGA and ASIC. Furthermore, in the context of analog design, I'm focused on Ultra Low Voltage and Ultra Low Power architectures for IoT interfaces, such as OTAs, Filters, LNAs, Comparators and Sense Amplifiers.

2019-2020

Master's degree in Electronic Engineering: Summa Cum Laude

"La Sapienza" University of Rome, Course in Information and Communication Technology (ICT)

My Master's degree thesis was focused on Physical Unclonable Function, both from an analog and a digital perspective. In the context of the analog design, I was focused on Regulated Cascode Current Mirrors, deepening in highly robust interface with respect to PVT variations. With respect to digital design on FPGA, I get into detail of Ultra Compact and Lightweight architectures, focusing on the Xilinx's FPGA.

2017-2018 **Bachelor's Degree in Electronic Engineering: Summa Cum Laude**

"La Sapienza" University of Rome, Course in Information and Communication Technology (ICT)

My Bachelor's degree thesis was focused on 6th order Butterworth filter for Neural Recording Applications, the project of the filter was also published in [1].

FUNDING INFORMATION

2021 **Investigator in Progetto Ateneo 2021, Progetto di circuiti integrati CMOS a bassissima tensione di alimentazione e a bassissimo consumo di potenza per sistemi biomedicali "impiantati" con particolare riferimento all'elaborazione dei segnali neurali e alla neuro-robotica.**

"La Sapienza" University of Rome, Course in Information and Communication Technology (ICT)

Program The project aims to develop ultra-low-voltage CMOS integrated circuits with minimal power consumption, specifically designed for implantable biomedical applications. The primary goal is the efficient real-time processing of neural signals. Particular emphasis is placed on integration within neuro-robotic systems for advanced neural control and stimulation.

Grant Value 13000€

2023 **Principal Investigator in Progetto di avvio alla ricerca 2023, Sviluppo di blocchi funzionali a bassissimo consumo per applicazioni biomedicali**

"La Sapienza" University of Rome, Course in Information and Communication Technology (ICT)

Program The project focused on the development of ultra-low-power circuit blocks for biomedical devices, with particular emphasis on comparators and transconductance operational amplifiers. The goal was to optimize performance in terms of power consumption and silicon area. The proposed solutions are intended for use in implantable systems for monitoring and processing bioelectrical signals.

Grant Value 2332€

2024 **Investigator in Progetto Ateneo 2024, Design of low-power CMOS integrated circuits with minimized area footprint for multi-channel closed-loop neural-recording and stimulation systems in the context of Adaptive Deep brain stimulation.**

"La Sapienza" University of Rome, Course in Information and Communication Technology (ICT)

Program The project focuses on the design of low-power, compact CMOS integrated circuits intended for multi-channel systems for neural recording and stimulation in closed-loop configurations. The work centers on the efficient integration of architectures for Adaptive Deep Brain Stimulation (aDBS). The objective is to enhance the accuracy and responsiveness of real-time stimulation while minimizing power consumption and silicon area.

Grant Value 9780€

2023 **Investigator in Progetto Ateneo 2023, Development and design of reconfigurable entropy sources to be used as unified PUF-TRNG primitives for lightweight Hardware Cryptography in IoT applications.**

"La Sapienza" University of Rome, Course in Information and Communication Technology (ICT)

Program The project involves the development and design of reconfigurable entropy sources, used as unified PUF-TRNG primitives for lightweight hardware cryptography in IoT applications. The activity focuses on optimizing the reliability and variability of entropy responses. The goal is to ensure secure, low-cost, and low-power solutions for resource-constrained devices.

Grant Value 9180€

RESEARCH ACTIVITIES

Physical Unclonable Functions

Physical Unclonable Functions (PUFs) are unique, non-replicable physical functions that exploit intrinsic manufacturing process variations in circuits to generate unique digital responses to specific input stimuli (challenges). These responses are unpredictable and nearly impossible to clone, even by an attacker with physical access to the device. PUFs are employed in cryptographic applications for hardware authentication, secret key generation, and the protection of communication protocols.

Research in this field focuses on the design of the physical entropy source—that is, the circuit mechanism responsible for generating the PUF's unique behavior. Due to its inherent nature, each circuit exhibits a non-reproducible digital fingerprint that can be reliably reproduced upon each challenge while remaining hidden when inactive. This makes PUFs particularly well-suited for cryptographic key protection, as the key is never explicitly stored in the system but is instead generated on demand, thereby reducing the attack surface.

Depending on the PUF type (e.g., arbiter PUF, ring oscillator PUF, SRAM PUF), the architecture can be efficiently integrated into both FPGA and ASIC platforms, offering a scalable and secure solution for embedded systems and devices with strict constraints in terms of area, power consumption, and reliability.

True Random Number Generators

True Random Number Generators (TRNGs) are generators of random numbers that leverage inherently unpredictable physical phenomena—such as thermal noise, shot noise, or device mismatch—to produce non-deterministic binary sequences. These sequences are essential in various hardware security domains, including authentication protocols, cryptographic key generation, and anti-counterfeiting mechanisms.

Research in this area primarily focuses on the design and characterization of the entropy source, which is the block responsible for generating unpredictability at the physical level. The main challenge lies in ensuring that the source produces high-entropy data that is consistently unpredictable and resilient to external interference or tampering.

The circuit implementation is typically complemented by an excitation and sampling system, which converts the analog behavior of the entropy source into a digital sequence of random bits. Depending on the nature of the entropy source used (e.g., metastable oscillators, ring oscillator jitter, amplified thermal noise), TRNGs can be implemented on both ASIC and FPGA platforms, offering scalability, integrability, and adaptability to a wide range of application contexts and required security levels.

Hardware Cryptography

Research in hardware cryptography focuses on analyzing and protecting against physical vulnerabilities associated with the practical implementation of cryptographic protocols and block ciphers. Unlike theoretical cryptography, which studies the mathematical robustness of algorithms, this field concentrates on how these algorithms are actually realized at the circuit level, with particular attention to the potential leakage of sensitive information through side-channel attacks, glitching, or fault injection attacks.

The objective is to identify and mitigate these physical weaknesses through the integration of reliable entropy sources and dedicated hardware blocks aimed at ensuring physical security and resilience, such as True Random Number Generators (TRNGs) and Physical Unclonable Functions (PUFs). These elements are designed to enhance the robustness of hardware implementations of cryptographic primitives, providing an additional layer of security against attacks not addressed in abstract threat models.

Ultra Low Voltage ed Ultra Low Power

The continuous miniaturization of CMOS technology, coupled with the growing proliferation of applications requiring extremely low power consumption—such as Internet of Things (IoT) nodes, biomedical devices, and wearable systems—has driven the development of compact circuits operating at ultra-low supply voltages (Ultra Low Voltage, ULV).

To achieve ultra-low power (ULP) operation, it is essential to employ specialized biasing techniques for MOS devices, such as deep-subthreshold operation, in order to minimize energy consumption and enable the use of extremely low supply voltages. However, operating at such low voltages ($\leq$ 0.3V) requires dedicated design approaches.

Currently, the most widespread solutions rely on using the body terminal as an input (body-driven technique) and adopting inverter-based design methodologies.

Operational Transconductance Amplifiers

The design of Operational Transconductance Amplifiers (OTAs) for Ultra Low Voltage (ULV) and Ultra Low Power (ULP) systems represents one of the most complex and advanced challenges in modern analog electronics. This task requires a careful balance between power consumption, dynamic performance, and robustness against variations in process, voltage, and temperature (PVT).

Research in this field primarily focuses on innovative biasing techniques and circuit architectures optimized to operate with supply voltages as low as 0.3 V, while still delivering solid performance when driving capacitive loads typical of biomedical applications and sensors (typically in the range of 1 pF to 200 pF).

Among the proposed solutions, body-driven topologies with gate biasing—often based on CMOS inverter structures—have attracted particular interest. These configurations offer a favorable trade-off between energy efficiency and operational robustness, proving capable of maintaining stable performance even under significant environmental or technological variations, all while minimizing power consumption.

Comparators

The design of comparators for Ultra Low Voltage (ULV) and Ultra Low Power (ULP) systems is a key research area in modern analog electronics, with applications in biomedical devices, smart sensors, and IoT nodes. The goal is to achieve high sensitivity and speed performance while maintaining extremely low power consumption, even at supply voltages below 0.3 V.

The most advanced solutions rely on modified StrongARM architectures, body-driven techniques, and synthesizable digital implementations using standard logic cells. These approaches help reduce device stacking, improve robustness against PVT variations, and simplify integration within digital design flows.

Research focuses on optimizing the trade-off between offset, power consumption, area, and input common-mode range (ICMR), making the comparator a critical component in ULV/ULP systems. In this context, the investigation has explored both body-driven designs and standard-cell-based approaches.

SUMMARY OF SCIENTIFIC ACHIEVEMENTS

As of May 19th, 2025, according to the Scopus database, I have 47 publications with a total of 545 citations and an h-index of 16.

- papers : 55 (Scopus Database, October 6th, 2025)
- journals : 33 (Scopus Database, October 6th, 2025)
- conferences : 22 (Scopus Database, October 6th, 2025)
- total citations : 680 (Scopus Database, October 6th, 2025)
- Hirish (H) index : 18 (Scopus Database, October 6th, 2025)

PERSONAL SKILLS

Mother tongue Italian

Other languages

	UNDERSTANDING		SPEAKING		WRITING
	Listening	Reading	Spoken interaction	Spoken production	
English	C1	C1	C1	C1	C1

Levels: A1 and A2: Basic user – B1 and B2: Independent user – C1 and C2: Proficient user
Common European Framework of Reference for Languages

Communication skills

Excellent communication and interpersonal skills including respect, empathy and clarity acquired through years of private teaching of Physics, Mathematics, Electronics and Computer Science for University and High School students.

Organisational / managerial skills

Good organizational and management skills acquired through years of sport accompanied by school studies and classical music. Determination, dynamism and resilience acquired through years of individual sports at a competitive level such as men's artistic gymnastics and modern pentathlon. Team spirit, adaptability and flexibility acquired through years of volleyball at a competitive level, playing up to the Serie D championships.

Job-related skills

- In-depth knowledge of Linux and Linux based operating systems including Ubuntu, Fedora, Red Hat, Arch-Linux, Debian, Chrome OS;
- Good knowledge of office programs such as Microsoft Office suites, OpenOffice, Libre Office;
- Excellent knowledge of LaTeX;
- Excellent knowledge of software tools for the design and analysis of electronic circuits such as the Orcad suite, Cadence, Modelsim, Vivado, Xilinx-ISE;
- Excellent programming skills with C, C ++, Bash, Python, TCL, Verilog, VHDL.

Research Awards and Recognitions

- In 2025 I was ranked among the top 2% of scientists worldwide, according to the list by Stanford University and Elsevier, more information about my current rank can be found here.
- The paper [5] entitled "0.3 V, Rail-to-Rail, Ultralow-Power, Non-Tailed, Body-Driven, Sub-Threshold Amplifier" has been selected among the top 20 cited papers in 2021 in the Section "Energy Science and Technology" of MDPI, link to the news: https://www.mdpi.com/about/announcements/5235.
- The paper [3] entitled "A 0.3 V, Rail-to-Rail, Ultralow-Power, Non-Tailed, Body-Driven, Sub-Threshold Amplifier" has resulted among the highly cited papers in Section "Energy Science and Technology" of Applied Sciences MDPI.
- The paper [23] won the gold leaf certificate (certificate for the top 10% papers) at the 18th International Conference on PhD Research in Microelectronics and Electronics (PRIME)

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